Protection of the Switches in a Three-Level Inverter by Using Modified Switching Schemes for the Redistribution of Losses

Von der Naturwissenschaftlich-Technischen Fakultät
der Universität Siegen

zur Erlangung des akademischen Grades

Doktor der Ingenieurwissenschaften
(Dr.-Ing.)

genehmigte Dissertation

von
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Tag der mündlichen Prüfung: **17.06.2016**

Vorwort

Die vorliegende Arbeit entstand während meiner Tätigkeit als Promotionsstudent am Institut für Leistungselektronik und Elektrische Antriebe der Universität Siegen.

Zuerst möchte ich Herrn Prof. Dr.-Ing. Mario Pacas für seine Unterstützung und für seine große Geduld danken. Er hat mir immer wieder wertvolle Anregungen sowie Motivation gegeben und dadurch entscheidend zum Gelingen der Arbeit beigetragen.

Für die Übernahme des Koreferats danke ich Herrn Prof. Dr.-Ing. Andreas Steimel von der Universität Bochum für seine akribischen Korrekturen meiner schriftlichen Arbeit sowie für seine anschauliche Erklärung der thermischen Modellbildung.

Herrn Prof. Dr. Mustafa Kizilcay danke ich für die Übernahme der Leitung des Promotionsverfahrens.

Bei Herrn Dr. Gernot Riedel und Herrn Dr. Nikolaos Oikonomou von ABB Corporate Research, Baden-Daettwil, Schweiz, möchte ich mich für Ihre zahlreichen wertvollen Fachdiskussionen während des Projekts bedanken.

Für die angenehme Zusammenarbeit und für den vielfältigen Wissensaustausch möchte ich mich auch bei den Mitarbeitern und Kollegen des Institutes bedanken: Herrn T. Othman, Frau S. Leukel, Herrn E. Oerter, Herrn W. Bruch, Herrn M. Steinbring, Herrn S. Feuersänger.

Nicht zuletzt danke ich meiner Familie, Verwandten und Freunden, die mich während der Forschungsarbeit stets unterstützen.

Siegen, den 16.11.2016

The Minh PHAN

Abstract

Switching devices (IGBT, IGCT, etc.) of **T**hree-level **N**eutral-**P**oint-**C**lamped **V**oltage **S**ource **I**nverters (3L-NPC-VSI) for high-power applications are typically mounted on dedicated heatsinks, which results in a lack of heat sharing among the switches. Several control strategies have been proposed to enable even distribution of losses among the switches in normal operation, however a local thermal overload can occur due to adverse operating conditions such as: degradation of cooling system, inappropriate placing of semiconductor device, failures in electronics, etc. The thermal overload increases the risk of thermal breakdown of the affected device and reduces consequently the expected lifetime of inverter.

A new fault-tolerant control approach is proposed in the work to deal with this matter. In case of thermal overload, the control method of inverter is immediately adapted, so that the stressed switch is relieved, the heat is distributed to the other devices which are not affected by the overload. Here, redundant states of multi-level inverter are taken advantage of, since redundancies of a voltage space vector deliver the same line-to-line output voltage, but having different impact on the loss distribution among the switches of the inverter. Thanks to the active redistribution of losses among the switches, the temperature of the affected device is kept under the critical limit. In this way, the lifetime of the inverter is maximized even in case of thermal overload.

The proposed strategy will be examined with two control methods for the inverter feeding an induction machine: **F**ields **O**riented **C**ontrol (FOC) and **D**irect **T**orque **C**ontrol (DTC), which are very widespread in the practice. The implementation of each control method requires different considerations and strategies. Finally, the impact of the optimized switching pattern on loss distribution among the switches will be verified by means of simulation and measurements on a laboratory set-up. During operation of the proposed control methods, the stability of the neutral-point potential of the inverter is ensured without any additional hardware.

Zusammenfassung

Elektronische Ventile (IGBT, IGCT, usw.) eines Drei-Punkt-Wechselrichters (3L-NPC-VSI) für Mittelspannungsanwendungen werden üblicherweise auf separaten Kühlkörpern montiert, als Folge entsteht eine schwache thermische Kopplung zwischen den Ventilen. Wie aus der Literatur bekannt ist, kann im normalen Betrieb des Wechselrichters die Wärmeverteilung zwischen den Schaltern mit Hilfe verschiedener Verfahren verbessert werden. Trotzdem ist die Entstehung von lokalen Hotspots unter bestimmten Fehlersituationen wie: Störung im Kühlsystem, schlechter Platzierung der Ventile, Fehler in der Elektronik usw. unvermeidbar. Die lokale thermische Überlastung erhöht das Ausfallrisiko der betroffenen Ventile und reduziert die Lebensdauer des gesamten Systems.

In der vorliegender Arbeit wird ein neuartiger fehlertoleranter Regelungsansatz entwickelt, um das Problem anzugehen. Im Falle der lokalen thermischen Überlastung wird die Pulsweitenmodulation bzw. werden die Schaltmuster so adaptiert, dass die thermisch belasteten Ventile geschont werden und ein Teil der Wärme auf andere, nicht überlastete Schalter verlagert wird. Dabei werden redundante Zustände des 3L-NPC-VSI ausgenutzt, welche dieselbe Ausgangsspannung haben, aber unterschiedlichen Einfluss auf die Verlustverteilung des Wechselrichters nehmen. Dank der aktiven Verlustverteilung zwischen den Ventilen bewegt sich der Temperaturwert der überlasteten Ventile im erlaubten Bereich und das System kann im Betrieb bleiben. Darüber hinaus wird die Lebensdauer des Wechselrichters selbst im Fehlerzustand maximiert.

Der vorgeschlagene Ansatz wird in zwei verschiedenen Varianten untersucht. Die erste betrachtet den 3L-NPC-VSI als Stellglied einer feldorientiert geregelten Asynchronmaschine und modifiziert die Pulsweitenmodulation entsprechend. Im zweiten Fall wird die Direkte Drehmomentregelung (DTC) betrachtet und die Schalttabelle modifiziert. Die vorgeschlagene fehlertolerante Prozedur minimiert auch ihre Auswirkungen auf die Mittelpunktspannung des Zwischenkreises, ohne dass zusätzliche Hardware notwendig ist. Das Verfahren wird mittels Simulation und zahlreicher Messungen an einem Laborprüfstand validiert.

Nomenclature

Notation

x	Small letter symbol stands for an AC quantity
X	Capital letter symbol stands for a DC quantity or rms. value
$\underline{x} = Re(\underline{x}) + j \cdot Im(\underline{x}) = \lvert\underline{x}\rvert \cdot e^{j \cdot \varphi_x}$	Space vector representation in the complex plane
$\hat{x}$	Magnitude of an AC quantity
$\lvert\underline{x}\rvert$	Magnitude of space vector $\underline{x}$
$\tilde{x}$	Peak-to-peak value of an AC quantity
$\bar{x}$	Average value of an AC quantity

Space vector quantities

$\underline{i}'_{R,dq}$	Rotor-current space vector in d,q-rotor flux oriented coordinate system
$\underline{i}'_R$	Rotor-current space vector
$\underline{i}_{S,dq}$	Stator-current space vector in d,q-rotor flux oriented coordinate system
$\underline{i}_{S,\alpha\beta}$	Rotor-current space vector in α,β-stator oriented coordinate system
$\underline{i}_S$	Rotor-current space vector
$\underline{u}_1, \underline{u}_2\ and\ \underline{u}_3$	Three nearest-voltage space vectors
$\underline{u}_{S,\alpha\beta}$	Stator-voltage space vector in α,β-stator oriented coordinate system
$\underline{u}_S$	Stator-voltage space vector
$\underline{u}_{i,\alpha'\beta'}$	(i =1, 2 or 3) Three nearest-voltage space vectors in oblique α',β'-coordinate system
$\underline{u}_{i,\alpha\beta}$	(i =1, 2 or 3) Three nearest-voltage space vectors in α,β-stator oriented coordinate system

$\underline{u}_i$	(i =1, 2 or 3) Three nearest-voltage space vectors (compact form)
$\underline{u}_{ref}$	Reference voltage space vector
$\underline{u}_{ref,\alpha'\beta'}$	Reference voltage space vector in oblique α', β'-stator oriented coordinate system
$\underline{\psi'}_{R,\alpha\beta}$	Rotor-flux linkage space vector in α, β-stator oriented coordinate system
$\underline{\psi'}_R$	Rotor-flux linkage space vector
$\underline{\psi}_{S,\alpha\beta}$	Stator-flux-linkage space vector in α, β-stator oriented coordinate system
$\underline{\psi}_S$	Stator-flux-linkage space vector

Capital letter symbols

E_{Switch}	Switching loss energy of semiconductor device
$L_{S,h}$	Mutual inductance
$L'_R = L'_{R,\sigma} + L_{S,h}$	Rotor inductance
$L'_{R,\sigma}$	Rotor leakage inductance
$L_{S,\sigma}$	Stator leakage inductance
$L_S = L_{S,\sigma} + L_{S,h}$	Stator inductance
M_i	Inner torque of induction machine
M_{load}	Load torque on rotor shaft
M_{rated}	Rated torque of induction machine
N_f	Number of cycles to failure
$P_{Loss,ALE}$	Losses of IGBT in Active Lifetime Extension (ALE) operation
$P_{Loss,DPWM}$	Losses of IGBT in discontinuous PWM operation
P_{Loss}	Losses of IGBT
R_{ca}	Thermal resistance of case to heatsink
R_{ha}	Thermal resistance of heatsink to ambient
S_U, S_V, S_W	Connection states of phases U, V and W of inverter, +

	refers connection of one phase to positive potential, - to negative DC rail, 0 to neutral point
$S_{i,U}, S_{i,V}, S_{i,W}$	Connection states of phases U, V and W of inverter using voltage space vector $\underline{u}_i$
ΔT_{ch}	Temperature difference between case and heatsink
ΔT_{jc}	Temperature difference between junction and case
ΔT_{ha}	Temperature difference between heatsink and ambient
T_S	Switching period or sampling period (interval)
U_{C1}, U_{C2}	Voltages of capacitors C1 and C2
U_d	Step voltage
U_{DC}	DC-link voltage of inverter
U_{GE}	Gate-emitter voltage of IGBT
U_{LL}	Line-to-line stator voltage of induction machine

Small letter symbols

c_i	Common-mode component of a switching state of voltage space vector $\underline{u}_i$ $(i = 1, 2, 3)$
$d_1, d_2\ and\ d_3$	Duty cycles of three nearest-voltage space vectors $\underline{u}_1, \underline{u}_2\ and\ \underline{u}_3$
$d_{S1,inverse}$	Duty cycle of redundant state, which connects two phases of inverter to neutral point
$d_{S1,non-inverse}$	Duty cycle of redundant state, which connects one phase of inverter to neutral point
f_S	Fundamental frequency of stator current
i_C	Collector current of IGBT
i_{NP}	Neutral-point current
$i_{S,U}, i_{S,V}\ and\ i_{S,W}$	Instantaneous values of stator currents of phase U, V and W
$i_{S,d}\ and\ i_{S,q}$	The d- and q-components of stator current in d, q-rotor-flux-oriented coordinates

$i_V, i_U \; and \; i_W$	Instantaneous values of current of phase U, V and W, respectively
m	Modulation index
n	Level of inverter
p	Number of pole pairs of machine
r_{CE}	Differential resistance
u_{CE}	On-state voltage drop across IGBT
u_{CMV}	Common-mode voltage or common-mode signals
$u_{NP} = U_{C1} - U_{C2}$	Neutral-point voltage
$u_{S,\alpha} \; and \; u_{S,\beta}$	α- and β-components of stator-voltage space vector in α, β-stator oriented coordinates
$u_{ref,U,mod}$, $u_{ref,V,mod}$, $u_{ref,U,mod}$	Reference voltage of phase U, V, W, respectively, with injection of common-mode signal
$u_{ref,U}$, $u_{ref,V}$, $u_{ref,W}$	Reference voltage of phase U, V and W, respectively
$u_{ref,\alpha} \; and \; u_{ref,\beta}$	α- and β-components of reference-voltage space vector in α, β-stator-oriented coordinates
$u_{ref,\alpha'} \; and \; u_{ref,\beta'}$	α'- and β'-components of reference-voltage space vector in 60° oblique α', β'-stator-oriented coordinates
$u_{i,\alpha'} \; and \; u_{i,\beta'}$	α'- and β'-components of voltage space vector $\underline{u_i}$ $(i = 1, \; 2, 3)$ in 60° oblique α', β'-stator-oriented coordinates
u_{tr}	Triangle carrier signal
u_{UN}, u_{VN}, u_{WN}	output voltage of phase U, V and W, respectively, in relation to neutral point of the DC-link voltage
δ_φ	Load angle
η	Lifetime extension factor
ω_R	Electrical angular speed of rotor
$\varphi_{\psi,R}$	Phase of rotor-flux-linkage space vector $\underline{\psi}_R$
ρ_i	Redundancy order of voltage space vector $\underline{u_i}$
σ	Leakage factor

σ_R	Leakage factor of rotor
σ_S	Leakage factor of stator
τ_R	Time constant of rotor
ϑ	Operational angle limiting the area, in which ALE strategy is applied
ξ	Weighting factor for neutral-point control by C-PWM

Acronyms

3L-NPC VSI	Three-level neutral-point-clamped voltage source in-
AC	Alternating Current
ADC	Analog to Digital converter
ALE	Active Lifetime Extension
CB-PWM	Carrier-based pulse width modulation
C-PWM	Continuous pulse width modulation
DAC	Digital to Analog converter
DC	Direct current
D-PWM	Discontinuous pulse width modulation
DSP	Digital Signal Processor
DTC	Direct Torque Control
EMI	Electromagnetic Interference
FOC	Field Oriented Control
IGBT	Insulated gate bipolar transistor
IM	Induction Machine
NP	Neutral point
PF	Power Factor
PI	Proportional-Integral controller
PWM	Pulse width modulation
SV	Space Vector
SV-PWM	Space vector pulse width modulation
THD	Total harmonic distortion
TNVs	Three nearest vectors to generate the reference voltage
VSI	Voltage source inverter

Contents

1 Introduction

1.1 Motivation

Nowadays, multilevel inverters are considered as the preferred choice for medium- and high-power applications as e.g. railway traction, high-voltage direct-current transmission, marine propulsion, rolling mills, compressors, etc. The multilevel inverters feature: Higher rated voltage, lower common-mode voltage, reduced dv/dt, near-sinusoidal output current; lower switching frequency, smaller input and output filter (if required), possible fault-tolerant operation, etc. However, this technology still presents a great number of challenges, which have to be improved in terms of efficiency, reliability, power density, cost, etc. [1]−[3].

One of the most widely used topologies for the medium-voltage drive application is the Three-level Neutral-Point-Clamped Voltage Source Inverter (3L-NPC VSI), which is offered by diverse manufacturers [4]−[5]. The advantages of a 3L-NPC VSI are: Common DC-bus configuration, net-friendly operation by means of small additional filters, simple inclusion of brake chopper, etc. [4]. However, one of the inherent drawbacks of this topology is the uneven loss distribution among the semiconductor devices, since the inner and outer switches are modulated in different manner. Furthermore, the loss differences of the used components can also worsen the heat distribution. In some extreme cases, a switch or a switching group may be exposed to thermal overload due to malfunction of the driver circuits, degradation of cooling system, inappropriate placing of switches, etc. Thus, the reliability of the inverter is significantly reduced, since the lifetime of an inverter is limited mostly due to the particular component suffering thermal overload. Therefore, the relieving of such local hotspot is strongly demanded.

1.2 Objective of research work

In multilevel inverters the output voltage are synthesized by applying different switching patterns. Yet in some cases, distinct switching patterns generate the same line-to-

line voltage and are therefore generating redundant states. In the conventional modulation techniques for 3L-NPC VSI, these redundancies are used for the balancing of the voltages in the capacitors of the DC link or for reducing the common-mode voltage of the inverter.

In this work, a new modulation strategy for 3L-NPC VSIs is proposed with the target to *actively* redistribute losses from the stressed device to the other switches by taking advantage of the redundancies of the output voltage [6]. Thanks to the loss redistribution, the risk of the thermal breakdown of the affected device can be reduced. As a long-term effect, the lifespan of inverter is improved considerably [6]. Therefore, this control strategy is called "Active Lifetime Extension" (**ALE**).

The proposed control concept is completely different from the proposals in [7]−[9]. There, the topology of the 3L-NPC VSC is modified by replacing the neutral-point diodes with IGBTs. In a conventional 3L-NPC VSI, if one output phase is connected to the neutral point, the phase current flows in a natural way through either the upper or the lower neutral-point diodes path, depending on the current sign. By employing IGBTs instead of diodes for the clamping to the neutral point, the current can be forced to flow through the upper or through the lower clamping path by turning on the appropriate IGBT(s). Thus, this topology is called Three-Level **Active**-Neutral-Point-Clamped VSI (3L-**A**NPC VSI) due to the active clamping of neutral point. Furthermore, four additional redundant states are obtained thanks to this modification. These additional redundancies of the output voltage are used to achieve an uniform distribution of losses among the switches of inverter. Hence, the approach and the target of the present work are completely different to those in [7]−[9].

In [10] a method for the thermal redistribution for the range of low modulation index and for ride-through condition is presented, that is likely similar to the proposal of the present work. There, the inverter is operated in the low modulation range while the current is reactive and the redundant states of the zero-voltage space vectors are used to relocate the losses. In the present work, not only the redundancies of the zero-voltage space vector, but also the redundancies of short voltage space vectors are used

for the redistribution of the losses. Moreover, the control is designed for operation in the whole ranges of modulation index and current of the inverter.

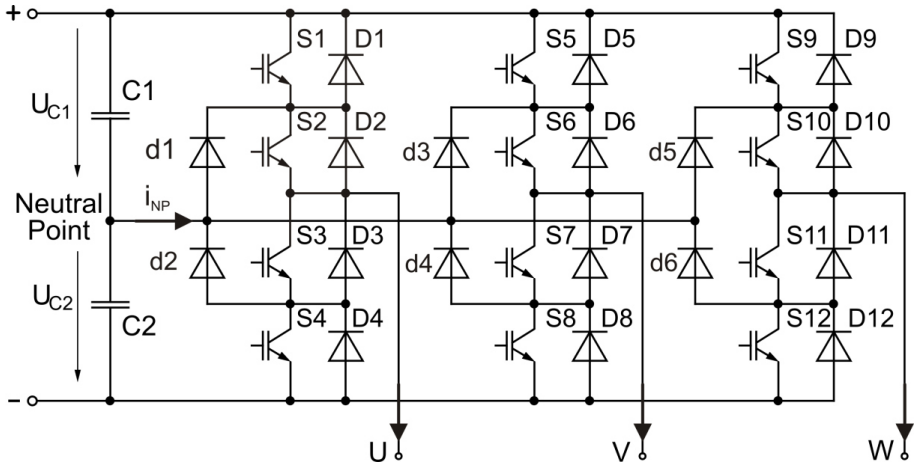


Figure 1: 3L-NPC Inverter, the neutral-point voltage is defined as $u_{NP} = U_{C1} - U_{C2}$

1.3 Problem formulation and contribution of this work

Without loss of generality, it is assumed that the switches S1 and S2 of phase U in Figure 1 are exposed to excessive thermal stress and these have to be relieved.

Thus, the following thesis can be formulated: "The losses of the affected switches S1 and S2 can be reduced by applying the ALE switching strategy that will be based on the proper utilization of the redundant states of the 3L-NPC-VSI and that will be developed in this work". The switching strategy to be developed has to take into account the impact of the pulse width modulation on the symmetric distribution of voltages in the DC link. This thesis has to be proven by means of simulation and experiments.

The switches of the laboratory set-up used to verify the PWM with ALE are mounted on dedicated heatsinks, since this ensures a thermal decoupling among the switches and simplifies the estimation of losses of each switch, as the temperature difference of the heat sink to ambient is directly proportional to the total losses in case of steady state.

The main contribution of this work will be a switching strategy that allows the redistribution of the thermal losses in a 3L-NPC VSI in case of overheating of one of the switches and that leads to an Active Life Time Extension (ALE) by keeping the temperature of the affected switch below the critical limit, without a relevant degradation of the voltage balancing in the DC link. The proposed PWM with ALE is not only useful for the 3L-NPC VSI, but also applicable for any kind of multilevel inverter topology to enable the active loss redistribution among the switching devices without the need of additional hardware.

1.4 Outline of thesis

The thesis is organized as follow: **Chapter 1** presents a brief introduction as well as the motivation of the research work. In **Chapter 2** some fundamentals used throughout the thesis including 3L-NPC VSI topology, space-vector theory, basics of the control methods for induction machines and the estimation of losses in semiconductor devices are given. The principles of space-vector modulation (SV-PWM), of continuous and discontinuous PWM, of control of the neutral-point voltage and of PWM with ALE are treated in **Chapter 3**. The experimental set-up and the measurement results that verify the SV-PWM with ALE are shown in **Chapter 4**. The results of simulations of the PWM with ALE are presented in **Chapter 5**. **Chapter 6** deals with the application of the ALE strategy in case of Direct Torque Control (DTC), the corresponding results of simulations that verify this variant of ALE are provided. Finally, the impact of the active redistribution of losses on the lifetime of inverter will be discussed in **Chapter 7**.

2 Fundamentals

2.1 Three-level Neutral-Point-Clamped Voltage Source Inverter

The 3L-NPC VSI is widely used for industrial applications in the voltage range of 2.3 kV to 6 kV [5]. This topology is considered as a further development of the two-level inverter by adding two IGBT/diode pairs and two diodes from the IGBT connection points of each phase leg to the neutral point to provide an additional zero output level. The topology of 3L-NPC VSI is depicted in Figure 1. The DC link is split into two voltages U_{C1} and U_{C2}, thus each switching device of inverter has to withstand, on principle, only half the voltage U_{DC} of the DC link. As consequence, the 3L-NPC VSI can be built with semiconductor devices with the same voltage ratings like in a two-level inverter and nevertheless achieve the double output voltage.

The output voltage of each phase of the 3L-NPC VSI referred to the neutral point of the DC link has three discrete values, $+0.5U_{DC}, 0$ and $-0.5U_{DC}$ depending on the switching pattern. For example in the phase U voltage in relation to the neutral point shown in Figure 1:

- **Positive output voltage $\boldsymbol{u_{UN} = +0.5U_{DC}}$:** If S1 and S2 are turned on, the others turned off.
- **Zero-output voltage $\boldsymbol{u_{UN} = 0}$:** If S2 and S3 are turned on, the others turned off.
- **Negative output voltage $\boldsymbol{u_{UN} = -0.5U_{DC}}$: :** If S3 and S4 are turned on, the others turned off.

In order to simplify the notation the switching states S_x in phase $\mathrm{x} = \mathrm{U, V, W}$ are designated as follows:

- for $\boldsymbol{u_{xN} = +0.5U_{DC}}$ as $S_x = 1$ or simply as $S_x = +$
- for $\boldsymbol{u_{xN} = 0}$ as $S_x = 0$

- for $\boldsymbol{u_{xN} = -0.5U_{DC}}$ as $S_x = -1$ or simply as $S_x = -$

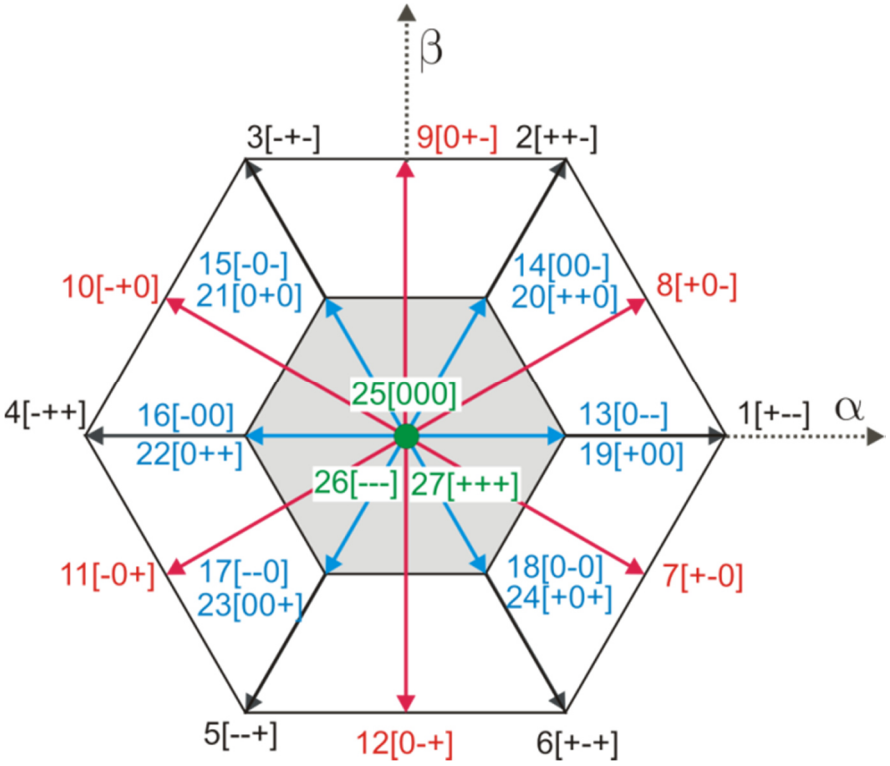


Figure 2: Space-vector diagram of 3L-NPC VSI comprising 19 voltage space vectors. The notation "+" refers to the connection of one phase to positive output potential, "0" to zero output potential and the "− " to negative output potential.

The 3L-NPC inverter can generate a total of $3^3 = 27$ switching combination. These states can deliver only 19 different voltage space vectors at the output of the inverter, which are shown in Figure 2 and can be classified into four groups:

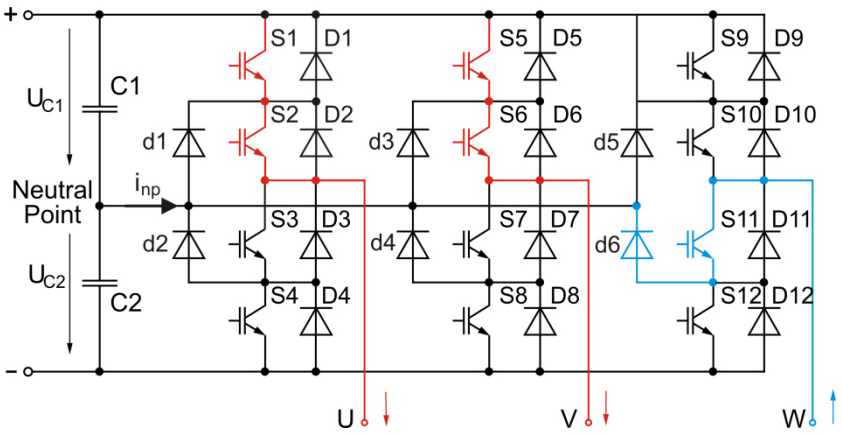
- **Long voltage space vectors:** The states depicted in black in Figure 2 have no redundant states and do not affect the neutral-point voltage of inverter.
- **Medium voltage space vectors:** The states depicted in red in Figure 2 exhibit no redundancies and distort the voltage balancing of the neutral point. They are the most important reason for the NP potential imbalance, especially for the operation in the range of high modulation index.
- **Short voltage space vectors:** The states depicted in blue in Figure 2 have each two redundancies, which can be used to reduce the imbalance of neutral-point voltage.

- **Zero-voltage space vector:** The states depicted in green in Figure 2 exhibit three redundant states that deliver a zero output voltage and have no effect on the neutral-point balancing.

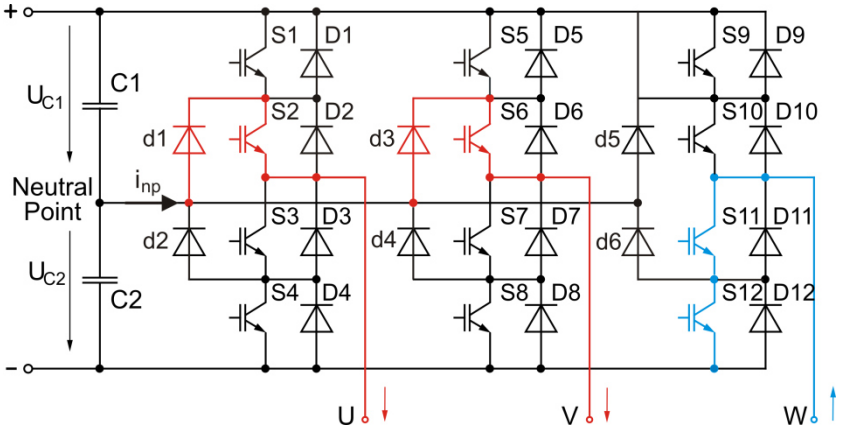
As mentioned above, the redundant states of a short voltage space vector (SV) come in pairs and each leads to different current paths. For example, Figure 3 shows the current flow in each phase of the inverter for the two different redundant switching states $[+\,+\,0]/[00-]$ applied to inverter. Obviously, the redundant states have different impact on the distribution of losses among the switches of inverter.

Regarding the balancing of the neutral-point voltage of the DC link, it can be seen in Figure 3 that the sign of the current flowing into the neutral point is not the same. In case of state $[+\,+\,0]$ the neutral-point current is given by $i_{NP} = i_W$, while in case of $[00-]$ the neutral-point current is expressed as $i_{NP} = i_U + i_V = -i_W$. Thus the capacitors $C1$ and $C2$ are charged and discharged in different manner depending on the use of the redundant switching states.

Furthermore, a pair of redundant switching states deliver different common-mode voltages, e.g. $[+\,+\,0]$ yields a positive common-mode voltage and it is called a *positive switching state*. In contrast, the state $[00-]$ is called *negative switching state* and produces a negative common-mode voltage. Here, the common-mode voltage of a switching state $[S_U\ S_V\ S_W]$ is defined as $u_{CMV} = \frac{S_U+S_V+S_W}{3}$. Among the four types of voltage space vectors, only the medium voltage space vectors e.g. $[-\,+\,0]$ delivers an effective common-mode voltage of zero. If medium voltage space vectors are favored to synthesize the output voltages, the common-mode voltage of the inverter can be reduced, but at the cost of higher distortion of the neutral-point voltage.



(a) Switching state [+ + 0]



(b) Switching state [00−]

Figure 3: The different impacts of redundant states delivering the same line-to-line voltage on the loss distribution among the switches of a 3L-NPC VSI

There are two main challenges for the application in the development of PWM with ALE for 3L-NPC VSIs that should be addressed in this early stage:

- First, during the operation of a 3L-NPC VSI, the redundant switching states of a short voltage space vector must be used alternatingly to ensure stability of neutral point. Unfortunately, the redundancies are also the only means used to redistribute the losses among the switches. For example, if S1 is exposed to excessive thermal stress, the use of e.g. [+ + 0] (see Figure 3 (a)) should be avoided in order to reduce the conduction losses of S1, and the switching state [00−] is to be used instead. Such operation affects the control of the neutral-point voltage. Therefore, a

tradeoff between the control of the neutral-point voltage and the active redistribution of losses has to be achieved.

- Secondly, the performance of the PWM with ALE depends strongly on the operating points of the inverter regarding modulation index and power factor. As a result, distinctive approaches have to be developed for the different operation index ranges.

2.2 Space vectors

The space-vector theory is widely used to describe three-phase systems under dynamical conditions [11] thru [13]. This provides great advantages, especially if the quantities of the three phases fulfill the condition $x_U + x_V + x_W = 0$, which is generally the case for currents in machines and networks with a free star point. The voltages fulfill also this condition, if the voltages are measured against the zero point. Thanks to this, only two quantities are linearly independent and the complex representation is useful:

$$\underline{x} = \frac{2}{3} \cdot \left(x_U + x_V \cdot e^{\frac{j2\pi}{3}} + x_W \cdot e^{\frac{j4\pi}{3}} \right) = x_\alpha + j \cdot x_\beta = \left| \underline{x} \right| \cdot e^{j \cdot \varphi_x}. \tag{1}$$

The coefficient 2/3 in the equations is a scaling factor, which reflects the fact that the quantities voltage, current and flux in a three-phase system UVW shall be represented in same size by an orthogonal two-phase coordinate system. The phase axes are defined by the unity space vectors 1, $e^{\frac{j2\pi}{3}}$ and $e^{\frac{j4\pi}{3}}$. Furthermore, the space vector $\underline{x}$ is determined by module $\left|\underline{x}\right|$ and phase angle φ_x in relation to an arbitrarily fixed coordinate axis. The instantaneous value of the quantity of each phase can be recalculated from the space vector $\underline{x}$ as:

$$x_U = Re(\underline{x}). \tag{2}$$

$$x_V = Re\left(\underline{x} \cdot e^{\frac{j2\pi}{3}}\right). \tag{3}$$

$$x_W = Re\left(\underline{x} \cdot e^{\frac{j4\pi}{3}}\right). \tag{4}$$

By using space vectors, the well-known voltage equations of the squirrel-cage induction machine in the stationary coordinate system can be written as:

$$\underline{u_S} = R_S \cdot \underline{i_S} + \frac{d}{dt}\underline{\psi_S}. \tag{5}$$

$$0 = R'_R \cdot \underline{i'_R} - \mathrm{j} \cdot \omega_R \cdot \underline{\psi'_R} + \frac{d}{dt}\underline{\psi'_R}. \tag{6}$$

Here, the notation x' means that a rotor quantity is referred to the stator side by taking into account the ratio of the number of turns in each system of windings [26]. R_S and $R_R^{'}$ are the stator resistance and rotor resistance, respectively. ω_R is the electrical angular frequency of the rotor. $\underline{\psi_S}$ and $\underline{\psi'_R}$ stand for the flux linkages of stator and rotor, respectively. The term $\mathrm{j} \cdot \omega_R \cdot \underline{\psi'_R}$ is required due to the transformation of the rotor voltage equation to the stationary coordinate system.

The relationship between the currents and fluxes are given by:

$$\underline{\psi_S} = \left(L_{S,h} + L_{S,\sigma}\right) \cdot \underline{i_S} + L_{S,h} \cdot \underline{i'_R}. \tag{7}$$

$$\underline{\psi'_R} = L_{S,h} \cdot \underline{i_S} + \left(L_{S,h} + L'_{R,\sigma}\right) \cdot \underline{i'_R}. \tag{8}$$

$$\sigma_S = \frac{L_{S,\sigma}}{L_{S,h}}, \sigma_R = \frac{L'_{R,\sigma}}{L_{S,h}}, \sigma = 1 - \frac{1}{(1+\sigma_S) \cdot (1+\sigma_R)}, \tag{9}$$

where σ_S and σ_R are the leakage factors of stator and rotor, respectively. $L_{S,\sigma}$ and $L_{R,\sigma}^{'}$ refer to the leakage inductances of stator and rotor. $L_{S,h}$ denotes the mutual inductance.

2.3 Modulation Techniques for 3L-NPC VSI

In the following the conventional PWM techniques including the carrier-based PWM and the Space-Vector modulation (SV-PWM) are introduced for the case of a 3L-NPC-Inverter. It will be shown how the degree of freedom resulting from the redundancy in the voltage space vectors can be used either for the reduction of the common-mode voltage or for the balancing of the neutral-point voltage, and finally how the newly developed PWM with ALE is included in the modulation scheme in order to obtain a redistribution of losses in the inverter in the case of a thermal overload in one of the semiconductor devices.

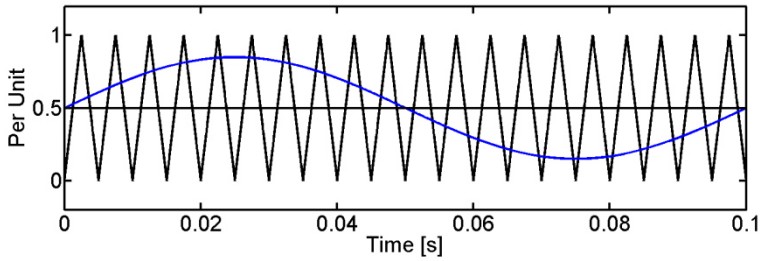
There are many different approaches for obtaining the switching patterns in a power electronic inverter. Apart from the generation of the switching pulses by using hysteresis controllers or model-based predictive or direct control techniques, the use of modulators is one of the most common solutions in industrial applications. The function of the pulse width modulator is the calculation of the switching patterns for the inverter from the desired output-voltage space vector by assuming a constant switching frequency.

Some well-known modulation techniques for the 3L-NPC VSI are among others: Selective Harmonic Elimination PWM (SHE-PWM), carrier-based PWM (CB-PWM) and space vector PWM (SV-PWM) [4]. SHE-PWM is regarded as a low-frequency modulation method and presents a very attractive solution for high-power applications due to its significant reduction of switching losses. Its implementation can often be cumbersome and requires extensive off-line calculations [16].

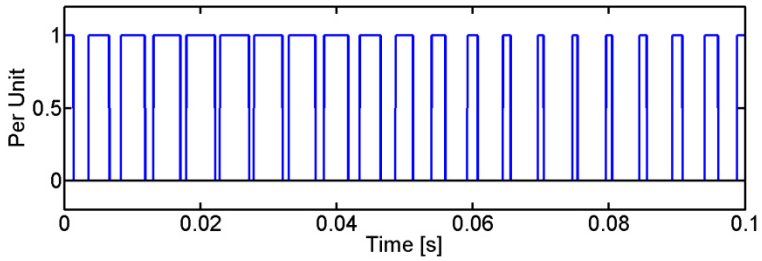
Conversely, CB-PWM and SV-PWM can be considered as high-frequency modulation techniques that feature excellent PWM quality. Since they are basic for the further understanding of the ALE, their principle will be presented in the next sections.

2.3.1 Carrier-based PWM (CB-PWM)

The **C**arrier-**B**ased (CB)-PWM also known as sine-triangle modulation is a standard and one of the oldest modulation technique for two-level inverters [13]–[15]. The principle of CB-PWM is illustrated in Figure 4 (a) for a two-level inverter, in which the modulation signal or the reference signal of the phase voltage u_{ref} is compared with the triangular carrier signal u_{tr} in order to generate the switching pattern to control the phase. The generated PWM signal of the upper switch in the half-bridge of the corresponding phase is shown in Figure 4 (b), where 1 and 0 refer to the turn-on and turn-off commands for the switch, respectively. This switch is turned on if $u_{ref} > u_{tr}$ and turned off for the case of $u_{ref} < u_{tr}$.



(a) Modulation of one phase of an inverter by comparing the reference signal u_{ref} (in blue) with the triangle signal u_{tr}



(b) Firing pulse of the upper switch of a phase, 1 refers to turn-on and 0 to turn-off

Figure 4: Generation of basic pulse pattern by using CB-PWM in a two-level inverter

Furthermore, the switching pattern for the lower switch is generated by inverting the switching pattern of the upper leg by adding a dead-time that considers the physical turn-off time of the switches.

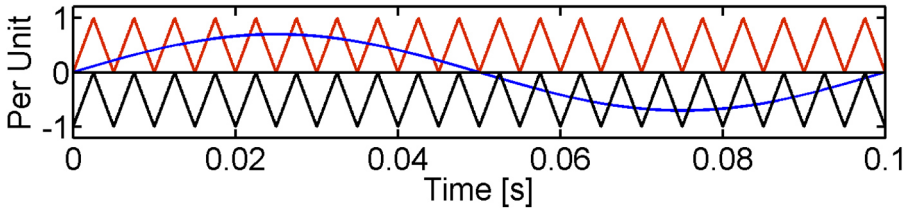
It can be shown that the CB-PWM can be enhanced by adding a common-mode function of triple fundamental frequency to the reference signal [17]. In this way an increase of the output phase voltage can be achieved. The adding of the common-mode signal corresponds to a zero-sequence [29] that in three-phase systems does not affect the current quality, since the injection of a zero-sequence voltage *does not alter* the line-to-line output voltages of an inverter.

The CB-PWM for the 3L-NPC VSI is an extension of the scheme explained above and is obtained by using an additional level-shifted triangular carrier signal.

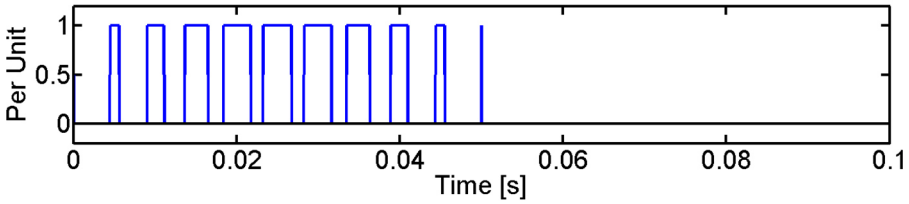
The reference voltage signals $u_{ref,U}$, $u_{ref,V}$ and $u_{ref,W}$ of the three phases are delivered by the current controllers and are typically sinusoidal in the steady state, as for instance the reference voltage signal $u_{ref,U}$ shown as blue curve in Figure 5 (a).

As example, the modulation of the switches in the phase U of the 3L-NPC inverter is presented in Figure 5. The PWM signals of the switches S1 and S2 (numbering refers to Figure 1) are shown in Figure 5 (b) and Figure 5 (c), respectively. In the first half period of u_{ref} the switch S1 is modulated and the switch S2 is kept turned on. The switch S1 is turned on if $u_{ref} > u_{tr1}$ and turned off for $u_{ref} < u_{tr1}$. When the reference signal u_{ref} becomes negative, the switch S1 is turned off and the switch S2 is modulated. Then switch S2 is turned on if $u_{ref} > u_{tr2}$ and turned off for $u_{ref} < u_{tr2}$.

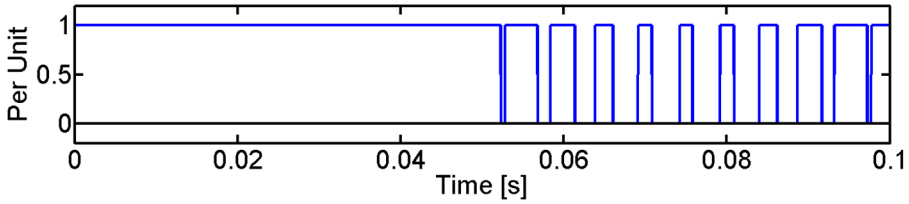
Because of the different switching patterns, the loss distribution among outer switches e.g. IGBT 1 and the inner switches e.g. IGBT 2 are not the same. The firing signals for S3 and S4 are generated by inverting the switching patterns of S1 and S2, respectively. The adding of dead-times to the PWM signals is in this case also required to prevent the short circuit.



(a) Modulation of phase U with reference signal $u_{U,ref}$ (blue curve), carrier signal u_{tr1} (in red) and carrier signal u_{tr2} (in black)



(b) Gate pulses of switch S1 of phase U, 1 refers to turn-on and 0 to turn-off



(c) Gate pulse of switch S2 of phase U, 1 refers to turn-on and 0 to turn-off

Figure 5: Generation of pulse pattern for phase U of 3L-NPC VSI

Like in the case of a two-level inverter, a zero-sequence signal u_{CMV} can be added to the reference voltage signals as (10). The modified reference signals of phase voltages $u_{ref,U,mod}$, $u_{ref,V,mod}$ and $u_{ref,W,mod}$ are no longer sinusoidal signals, moreover they contain harmonics with orders which are multiples of 3 and therefore they do not appear in the line-to-line voltage.

$$\begin{cases} u_{ref,U,mod} = u_{ref,U} + u_{CMV} \\ u_{ref,V,mod} = u_{ref,V} + u_{CMV} \\ u_{ref,W,mod} = u_{ref,W} + u_{CMV}. \end{cases} \tag{10}$$

The zero-sequence signal u_{CMV} has to be chosen in such way, that the reference voltage signals always satisfy the conditions (11):

$$\begin{cases} -1 \leq u_{ref,U,mod} \leq 1 \\ -1 \leq u_{ref,V,mod} \leq 1 \\ -1 \leq u_{ref,W,mod} \leq 1. \end{cases} \tag{11}$$

With a proper use of the zero-sequence signals, the 3L-NPC VSI operates in the linear range of the modulation index and the quality of the load current is not affected. The manipulation of the common-mode signal u_{CMV} presents an additional degree of freedom in the control scheme. Thus, it can be used for different control targets: redistribution of losses, reduction of common-mode voltage, balancing of the neutral-point voltage [31]−[33], etc.. CB-PWM is suitable for analog technique allowing a simple implementation. For the application of PWM with ALE on a 3L-NPC VSI, the control of the neutral-point voltage and the redistribution of losses have to be taken into consideration by manipulating the common-mode signal u_{CMV}.

2.3.2 Space-vector PWM (SV-PWM)

The **S**pace-**V**ector **P**ulse **W**idth **M**odulation (SV-PWM) is a modulation technique suitable for implementation on a digital control platform. It features a good utilization of the DC-link voltage and an easy optimization of the switching pattern at the cost of higher implementation effort, as compared with CB-PWM. The reference-voltage space vector $\underline{u}_{ref}$ delivered by the current controller is synthesized by using the three nearest-voltage space vectors $\underline{u}_1$, $\underline{u}_2$ and $\underline{u}_3$ that can be delivered by the inverter , forming the vertices of the triangle in the complex $\alpha, \beta -$ frame of coordinates, in which the reference-voltage space vector is located at the moment of sampling as in Figure 6.

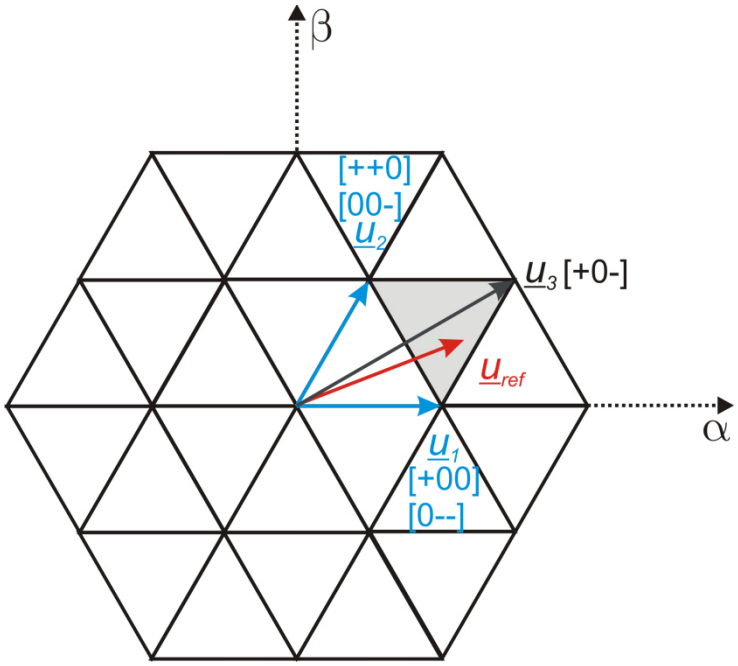


Figure 6: Synthesizing of the reference-voltage space vector $\underline{u}_{ref}$ with SV-PWM. The three nearest-voltage space vectors $\underline{u}_1$, $\underline{u}_2$ and $\underline{u}_3$ constitute the vertices of the shaded triangle

By assuming that for the switching period T_s the *voltage-time integral* of the desired output-voltage space vector is equal to the sum of *the voltage-time integrals* of the adjacent space vectors follows:

$$\underline{u}_{ref} \cdot T_s = (d_1 \cdot \underline{u}_1 + d_2 \cdot \underline{u}_2 + d_3 \cdot \underline{u}_3) \cdot T_s. \tag{12}$$

Being d_1, d_2 and d_3 the duty cycles of $\underline{u}_1$, $\underline{u}_2$ and $\underline{u}_3$, respectively, must yield:

$$d_1 + d_2 + d_3 = 1. \tag{13}$$

In fact, the average value of the voltage generated by the three nearest vectors has to be equal to the average value of the reference-voltage space vector over the sample period T_s as seen in (12). This is the basic principle for the well-known modulation techniques. Figure 6 shows a reference-voltage space vector, which is located in the shaded triangle together with the three nearest vectors $\underline{u}_1[+00]/[0--]$, $\underline{u}_2[++0]/[00-]$, $\underline{u}_3[+0-]$.

In the next section, the general SV-PWM algorithm for a n-level inverter will be presented. This algorithm was optimized to ease the implementation and the computation effort.

2.3.3 SV-PWM for a *n*-level VSI

The general algorithm of SV-PWM for a multilevel inverter comprises four stages:

- Identification of the three nearest-voltage space vectors (TNV) $\underline{u}_1$, $\underline{u}_2$ and $\underline{u}_3$ and computation of the corresponding duty cycles d_1, d_2 and d_3.
- Determination of the switching states of the TNV.
- Generation of the switching pattern.
- Generation of the PWM signals.

For the development of the PWM algorithm it is assumed that each phase of a $n-level$ inverter generates n discrete output voltages referred to the neutral point of the DC link: $-\frac{n-1}{2}U_d$, $-\frac{n-3}{2}U_d$, $-\frac{n-5}{2}U_d$, …, 0, …, $\frac{n-5}{2}U_d$, $\frac{n-3}{2}U_d$, $\frac{n-1}{2}U_d$. The step voltage U_d is calculated as $U_d = \frac{U_{DC}}{n-1}$.

Furthermore, the switching state $[S_U \quad S_V \quad S_W]$ is defined that describes the output voltage in each of the three phases as a function of the step voltage U_d in an easy way i.e.: $u_{UN} = S_U \cdot U_d$, $u_{VN} = S_V \cdot U_d$ and $u_{WN} = S_W \cdot U_d$. Here S_U, S_V and S_W are integer values, which fulfill the conditions: $-\frac{n-1}{2} \leq S_U, S_V \; and \; S_W \leq \frac{n-1}{2}$.

2.3.3.1 Identification of three nearest vectors

The space-vector diagram of an n-level inverter in the $\alpha, \beta -$ complex plane consists of six sectors, each comprising $(n-1)^2$ triangles. Thus, the determination of the triangle including the tip of the reference-voltage space vector among the many triangles is not a simple task. Various researchers have proposed different algorithms to reduce the computational effort of this task [34]–[39]. In the following, an identification procedure that is based on the method proposed in [39] will be explained.

The three phase reference voltages $u_{ref,U}$, $u_{ref,V}$ and $u_{ref,W}$ for the three phases U, V and W are transformed to the orthogonal $\alpha,\beta-$ complex plane or the stator-oriented coordinate system by using the well-known transformation:

$$\begin{bmatrix} u_{ref,\alpha} \\ u_{ref,\beta} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & \frac{\sqrt{3}}{3} & \frac{\sqrt{3}}{3} \end{bmatrix} \begin{bmatrix} u_{ref,U} \\ u_{ref,V} \\ u_{ref,W} \end{bmatrix}. \tag{14}$$

To simplify the identification of the three nearest vectors, the reference voltages $u_{ref,\alpha}$ and $u_{ref,\beta}$ are normalized with the step voltage $U_d = \frac{U_{DC}}{n-1}$ as a base quantity and are further transformed to an 60° oblique α',β'-coordinate system:

$$\begin{bmatrix} u_{ref,\alpha'} \\ u_{ref,\beta'} \end{bmatrix} = \frac{1}{U_d} \begin{bmatrix} 3/2 & -\sqrt{3}/2 \\ 0 & \sqrt{3} \end{bmatrix} \begin{bmatrix} u_{ref,\alpha} \\ u_{ref,\beta} \end{bmatrix}. \tag{15}$$

The reference-voltage space vector in the α',β'-coordinate system is expressed as $\underline{u}_{ref,\alpha'\beta'} = u_{ref,\alpha'} + j \cdot u_{ref,\beta'}$. The functions $Ceil$ and $Floor$ are referred to the **Nearest Integers Greater Than** and the **Nearest Integer Less Than**, e.g. $Ceil(2.4) = 3$ and $Floor(2.4) = 2$. Now, the three nearest vectors $\underline{u}_{1,\alpha'\beta'} = u_{1,\alpha'} + j \cdot u_{1,\beta'}$, $\underline{u}_{2,\alpha'\beta'} = u_{2,\alpha'} + j \cdot u_{2,\beta'}$ and $\underline{u}_{3,\alpha'\beta'} = u_{3,\alpha'} + j \cdot u_{3,\beta'}$ in the oblique α',β'-coordinate system can be easily identified as:

$$\begin{aligned} &if \quad (u_{ref,\alpha'} + u_{ref,\beta'} - \left(Ceil(u_{ref,\alpha'}) + Floor(u_{ref,\beta'})\right) > 0 \\ &\qquad \underline{u}_{3,\alpha'\beta'} = Ceil(u_{ref,\alpha'}) + j \cdot Ceil(u_{ref,\beta'}) \\ &\qquad \underline{u}_{2,\alpha'\beta'} = \underline{u}_{3,\alpha'\beta'} - j \\ &\qquad \underline{u}_{1,\alpha'\beta'} = \underline{u}_{3,\alpha'\beta'} - 1 \\ &else \\ &\qquad \underline{u}_{3,\alpha'\beta'} = Floor(u_{ref,\alpha'}) + j \cdot Ceil(u_{ref,\beta'}) \\ &\qquad \underline{u}_{2,\alpha'\beta'} = \underline{u}_{3,\alpha'\beta'} + j \\ &\qquad \underline{u}_{1,\alpha'\beta'} = \underline{u}_{3,\alpha'\beta'} + 1 \\ &end. \end{aligned} \tag{16}$$

The advantage of these transformations is that the real and the imaginary parts of the three resulting voltage space vectors $\underline{u}_{1,\alpha'\beta'}, \underline{u}_{2,\alpha'\beta'}$ and $\underline{u}_{3,\alpha'\beta'}$ are represented as integer numbers and in this way the computation effort can be reduced.

The corresponding duty cycles of the three nearest vectors obtained from (16) can be computed as (17).

$$
\begin{aligned}
&if \quad (u_{ref,\alpha'} + u_{ref,\beta'} - \left(Ceil(u_{ref,\alpha'}) + Floor(u_{ref,\beta'})\right) > 0 \\
&\qquad d_1 = \left|Im(\underline{u}_{3,\alpha'\beta'} - \underline{u}_{ref,\alpha'\beta'})\right| \\
&\qquad d_2 = \left|Re(\underline{u}_{3,\alpha'\beta'} - \underline{u}_{ref,\alpha'\beta'})\right| \\
&\qquad d_3 = 1 - d_1 - d_2 \\
&else \\
&\qquad d_1 = \left|Re(\underline{u}_{3,\alpha'\beta'} - \underline{u}_{ref,\alpha'\beta'})\right| \\
&\qquad d_2 = \left|Im(\underline{u}_{3,\alpha'\beta'} - \underline{u}_{ref,\alpha'\beta'})\right| \\
&\qquad d_3 = 1 - d_1 - d_2 \\
&end.
\end{aligned}
\tag{17}
$$

The general expression for the nearest-voltage space vectors $\underline{u}_{1,\alpha'\beta'}$, $\underline{u}_{2,\alpha'\beta'}$ and $\underline{u}_{3,\alpha'\beta'}$ is given as $\underline{u}_{i,\alpha'\beta'} = u_{i,\alpha'} + j \cdot u_{i,\beta'}(\mathrm{i} = 1, 2, 3)$ and their components $u_{i,\alpha'}$ and $u_{i,\beta'}$ are integer numbers and dimensionless.

2.3.3.2 Determination of switching states of three nearest vectors

The switching states $[S_{i,U} \quad S_{i,V} \quad S_{i,W}]$ of a particular voltage space vector $\underline{u}_{i,\alpha'\beta'}(\mathrm{i} = 1, 2, 3)$ of the three nearest vectors yield following relationship:

$$
\begin{aligned}
S_{i,U} &= u_{i,\alpha'} + u_{i,\beta'} + c_i \\
S_{i,V} &= u_{i,\beta'} + c_i \\
S_{i,W} &= c_i.
\end{aligned}
\tag{18}
$$

The difference between the redundant switching states of a given voltage space vector is in fact the common-mode voltage, thus the integer c_i in (18) is needed that reflects the common-mode part of a particular switching state $[S_{i,U} \quad S_{i,V} \quad S_{i,W}]$ and offers a degree of freedom. In order to determine the number of switching states to be found, the redundancy order ρ_i of a voltage space vector $\underline{u}_{i,\alpha'\beta'}$ is introduced here. In case of the 3L-NPC VSI inverter, if $\underline{u}_{i,\alpha'\beta'}$ is a short voltage space vector then it has a redundancy order of $\rho_i = 2$, thus two switching states have to be found. If $\underline{u}_{i,\alpha'\beta'}$ is a long or medium voltage space vector (as defined in 2.1) and thus non-redundant, then it has

a redundancy order of $\rho_i = 1$. The redundancy order ρ_i of a given voltage space vector $\underline{u}_{i,\alpha'\beta'} = u_{i,\alpha'} + j \cdot u_{i,\beta'}$(i = 1, 2 or 3) is defined as follows:

$$\begin{aligned} &if && u_{i,\alpha'} \cdot u_{i,\beta'} \leq 0 \\ &&& \rho_i = n - \max(|u_{i,\alpha'}|, |u_{i,\beta'}|) \\ &else \\ &&& \rho_i = n - |u_{i,\alpha'}| - |u_{i,\beta'}| \\ &end. \end{aligned} \tag{19}$$

The term *n* refers to the number of inverter levels, e.g. for a 3L-NPC VSI *n* = 3, the terms $u_{i,\alpha'}$ and $u_{i,\beta'}$ are integer numbers as in (16). With (19), the redundancy orders of each voltage space vector $\underline{u}_1$, $\underline{u}_2$ and $\underline{u}_3$ in the vertices of the triangles in the space-vector diagram can be found.

The calculation of the switching states is carried out by trying different values of c_i. The start value of c_i is set as $c_{i,old} = -\frac{(n-1)}{2}$. The switching state is then obtained by means of (18). Yet it is only valid if all the following conditions are fulfilled:

$$\begin{cases} -\dfrac{(n-1)}{2} \leq S_{i,U} \leq \dfrac{(n-1)}{2} \\ -\dfrac{(n-1)}{2} \leq S_{i,V} \leq \dfrac{(n-1)}{2} \\ -\dfrac{(n-1)}{2} \leq S_{i,W} \leq \dfrac{(n-1)}{2}. \end{cases} \tag{20}$$

If these three conditions are not satisfied, then the next value is tried by choosing$c_{i,new} = c_{i,old} + 1$. This new value $c_{i,new}$ is set again into (18) and the conditions (20) are examined. This search procedure will be continued until the *all three* conditions are satisfied and the first switching state of the voltage space vector $\underline{u}_{i,\alpha'\beta'}$ has been found.

If the voltage space vector $\underline{u}_{i,\alpha'\beta'}$ is a *non-redundant* voltage space vector, the search delivers only one switching state. In case $\underline{u}_{i,\alpha'\beta'}$ is a *redundant* voltage space vector, the search procedure continues and a value $c_{i,new} = c_{i,old} + 1$ is set until all redundant states are found.

2.3.3.3 Choice of proper switching sequence

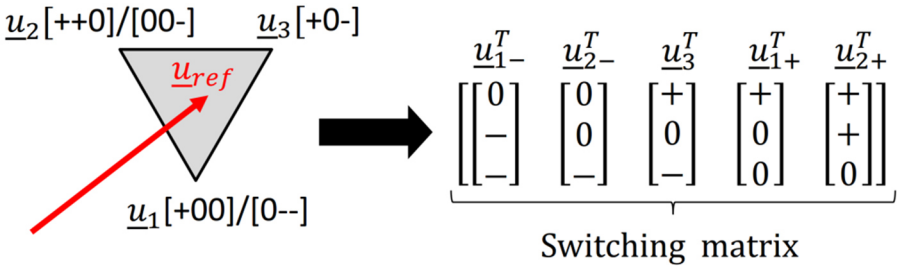


Figure 7: Arrangement of the switching states $[S_{i,U}\ S_{i,V}\ S_{i,W}]$ of the three nearest vectors in a switching matrix

Once the determination of the three nearest-vectors (TNVs), of the corresponding duty cycles and of the switching states has been accomplished as explained in the previous section, the next step for the realization of the SV-PWM is the generation of the switching sequence (switching pattern), which is required prior to the generation of the PWM signals at hardware level. Switching sequence or switching pattern is a set of consecutive switching states of the TNVs that together with their corresponding duty cycles are used for the generation of the switching signals or commands for the inverter. The placement of switching states has to be examined carefully in order to achieve minimal switching losses. For this purpose, the switching states found according to the procedure explained above in 2.3.3.2 are arranged in a switching matrix in such way that each switching state $[S_{i,U}\ \ S_{i,V}\ \ S_{i,W}]$ of the voltage space vector $\underline{u}_{i,\alpha'\beta'}$(i = 1, 2 or 3) builds a column of the matrix. The columns are ordered from left to right for an increasing value of the common-mode voltage of each state $u_{CMV} = \frac{1}{3}(S_{i,U} + S_{i,V} + S_{i,W})$. In such an arrangement the transition between two adjacent switching states demands only one switching action.

Figure 7 shows the switching matrix for the case that the reference-voltage space vector is located within the triangle with the vertices corresponding to the switching states $[1\ 0\ 0]$ $[0\ -1\ -1]$, $[1\ 1\ 0]$, $[0\ 0\ -1]$, $[1\ 0\ -1]$. According to the writing convention the values $(-1, 0, 1)$ of the switching states $[S_{i,U}\ S_{i,V}\ S_{i,W}]$ are written as $(-,0,+)$. In addition, the space vectors with a positive common-mode voltage are labeled with $+$ and those with a negative common-mode voltage with $-$, e.g. $\underline{u}_{2+}$ is a redundant

state with positive common-mode voltage whereas $\underline{u_2}_-$ has a negative one of the voltage space vector $\underline{u_2}$.

2.3.3.4 Generation of PWM signals

Finally, the switching sequence is used to generate the gate pulses to control the switches of the inverter.

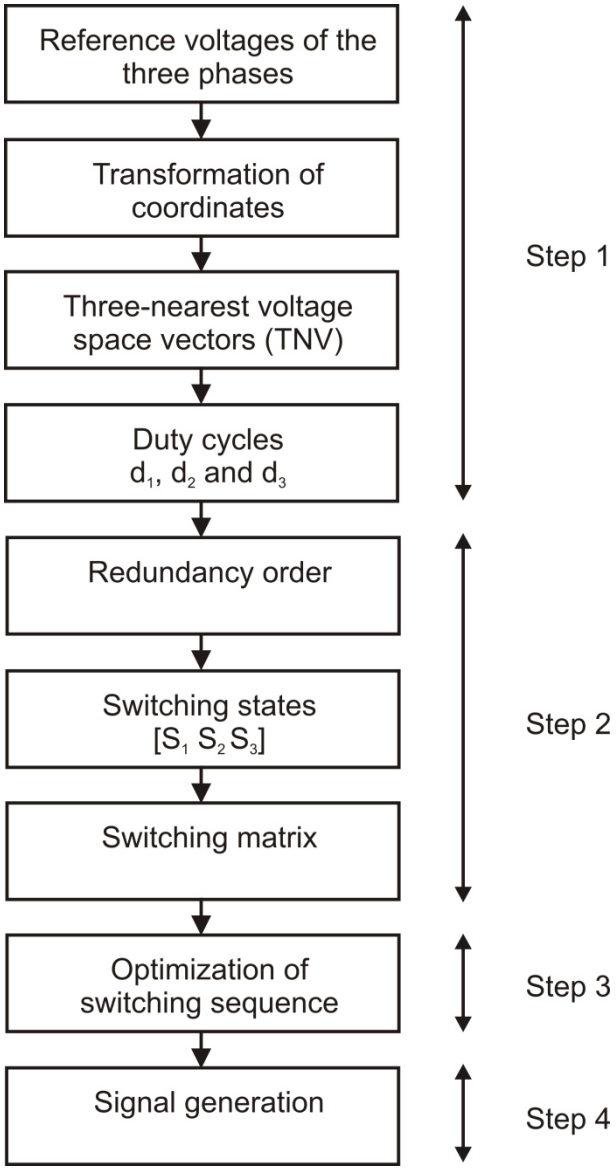


Figure 8: SV-PWM procedure for a n-level inverter

Figure 8 summarizes the implementation scheme of the general SV-PWM algorithm. **Step 1** and **step 2** are general for any type of n-level inverter. **Step 4** depends on the utilized hardware. Due to the presence of redundancies, different switching patterns

can be generated to synthesize the same reference-voltage space vector in **step 3**. The generation of switching patterns is considered as a degree of freedom in the control that can be used for different purposes such as: reduction of common-mode voltage, reduction of neutral-point voltage imbalance in case of 3L-NPC VSI, reduction of losses, etc. Thus, in the present work, this degree of freedom offered by SV-PWM will be the base for the realization of the PWM with ALE and therefore the next sections are dedicated to a comprehensive examination of the optimization of the switching sequences.

2.4 Generation of switching sequence

As explained above, the three nearest-voltage space vectors $\underline{u}_1$, $\underline{u}_2$ and $\underline{u}_3$ are used to synthesize the reference-voltage space vector, thus the switching sequence to be realized has to contain at least one switching state of each voltage space vector.

In case of the so-called discontinuous pulse width modulation (D-PWM) technique, a subset of *three* switching states is selected from the switching matrix to build the switching sequence for the sampling period.

The other possibility is the continuous pulse width modulation PWM (C-PWM) technique, in which four switching states are employed to form the switching sequence.

In fact, the switching matrix can contain more than four switchings and hence a subset of more than four switching states is also possible; however this implies higher switching losses and is not always favored in practice. In the next sections, the principle of C-PWM and of D-PWM will be discussed in the detail and illustrated for the case of the 3L-NPC VSI.

2.4.1 Continuous PWM

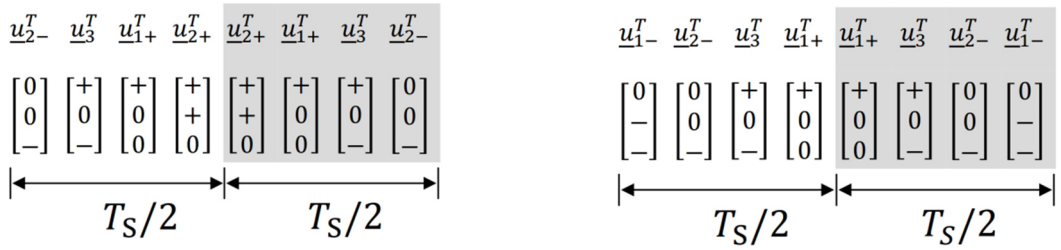
As stated above in case of continuous PWM, four switching states are selected from the switching matrix for building the switching sequence. According to (12), without loss of generality, the desired output-voltage space vector can be written:

$$\underline{u}_{ref} = \xi \cdot d_1 \cdot \underline{u}_{1-} + d_2 \cdot \underline{u}_2 + d_3 \cdot \underline{u}_3 + (1-\xi) \cdot d_1 \cdot \underline{u}_{1+}. \quad (21)$$

Here, the weighting factor ξ has been introduced and has to satisfy $0 \leq \xi \leq 1$ in order to fulfil (12). The switching sequence corresponding to (21) starts with switching state $\underline{u}_{1-}$ (redundant state with negative common-mode voltage) and ends with switching state $\underline{u}_{1+}$ (redundant state with positive common-mode voltage). Here the voltage space vector $\underline{u}_1$ plays a role of a **fictive** zero-voltage space vector and is called **pivot** zero-voltage space vector. This is similar to the case of the SV-PWM for a two-level inverter, in which the switching states of the active voltage space vectors are placed between the two redundant switching states of the zero-voltage space vector. The voltage space vectors $\underline{u}_2$ and $\underline{u}_3$ take the role of the active voltage space vectors. For the case $\xi > 0.5$, the negative redundant state $\underline{u}_{1-}$ is more favored than its positive counterpart $\underline{u}_{1+}$, as a result the contribution of the redundant switching states to the common-mode voltage is negative. In case of $\xi < 0.5$, the switching sequence leads to a positive of the redundant states to the common-mode voltage. Based on this consideration, the neutral-point voltage of the inverter can be controlled by means of varying the weighting factor ξ.

The best total harmonic distortion (THD) is obtained by choosing $\xi = \xi_0 = 0.5$, however the ripple of the neutral-point voltage is increased.

The role as pivot zero-voltage space vector can be taken by any of the voltage space vectors having redundant states, while the other two space vectors are considered as active voltage space vectors.



(a) Switching sequence

$$\underline{u}_{ref} = \xi \cdot d_2 \cdot \underline{u}_{2-} + d_3 \cdot \underline{u}_3 + d_1 \cdot \underline{u}_{1+} + (1-\xi) \cdot d_2 \cdot \underline{u}_{2+}.$$

(b) Switching sequence

$$\underline{u}_{ref} = \xi \cdot d_1 \cdot \underline{u}_{1-} + d_2 \cdot \underline{u}_{2-} + d_3 \cdot \underline{u}_3 + (1-\xi) \cdot d_1 \cdot \underline{u}_{1+}.$$

Figure 9: Examples of different switching sequences in C-PWM

In order to minimize the number of switching actions in the inverter, the switching sequences each switching period T_S is split in two consecutive identical sub-periods $T_S/2$ periods, the placement of the switching states of the second sub-period being a reversal of the arrangement in the first sub-period. The switching sequences depicted in Figure 9 (a) and (b) produce the same line-to-line output voltages. The explanations above make clear that manipulation of weighting factor ξ and the choice of different switching sequences offer additional degrees of freedom that can be used for different control purposes.

2.4.2 Discontinuous PWM

In case of discontinuous PWM [17] thru [19], three states of the switching matrix are chosen for building the switching sequence; they should be located in the matrix next to each other in order to reduce the number of switching actions. Again the output voltage is given as (12). In contrast to (21) for each of the three voltage space vectors in the vertices of the triangle, only one switching state is used. Nevertheless due to the redundant states, several switching sequences can be generated, each one resulting in a different common-mode voltage. In the example shown in Figure 7, three different cases are possible:

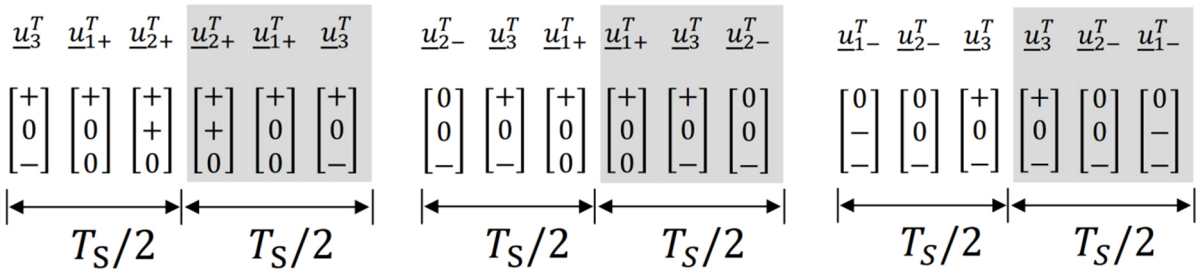
$$\underline{u}_{ref} = d_3 \cdot \underline{u}_3 + d_1 \cdot \underline{u}_{1+} + d_2 \cdot \underline{u}_{2+}. \quad (22)$$

$$\underline{u}_{ref} = d_2 \cdot \underline{u}_{2-} + d_3 \cdot \underline{u}_3 + d_1 \cdot \underline{u}_{1+}. \quad (23)$$

$$\underline{u}_{ref} = d_1 \cdot \underline{u}_{1-} + d_2 \cdot \underline{u}_{2-} + d_3 \cdot \underline{u}_3. \quad (24)$$

The switching sequence (22) is the **most positive** in terms of common-mode voltage as its contribution to the common-mode voltage is the highest of all three. In the same way, (24) can be considered to be **most negative** one.

Hence, the different sequences can be applied in alternated way to control the neutral-point voltage in case of a 3L-NPC VSI.



(a) Switching sequence (b) Switching sequence (c) Switching sequence

$\underline{u}_{ref} = d_3 \cdot \underline{u}_3 + d_1 \cdot \underline{u}_{1+} + d_2 \cdot \underline{u}_{2+}$

Clamping phase U to positive DC rail

$\underline{u}_{ref} = d_2 \cdot \underline{u}_{2-} + d_3 \cdot \underline{u}_3 + d_1 \cdot \underline{u}_{1+}$

Clamping phase V to neutral point

$\underline{u}_{ref} = d_1 \cdot \underline{u}_{1-} + d_2 \cdot \underline{u}_{2-} + d_3 \cdot \underline{u}_3$

Clamping phase W to negative DC rail

Figure 10: Placement of switching states in a switching sequence by D-PWM technique

Figure 10 (a) shows the placement of switching states of the switching sequence (22). It can be seen that during the whole switching period phase U of the inverter remains clamped to the positive DC rail and is not switched. Therefore, this technique is called discontinuous PWM. In case of the switching sequence (23), phase V is clamped to the neutral point of the inverter and the placement of switching states is shown in Figure 10 (b). Figure 10 (c) depicts the case (24), where phase W is clamped to negative DC rail.

2.5 Optimization of switching sequence aiming at reduction of neutral-point voltage imbalance

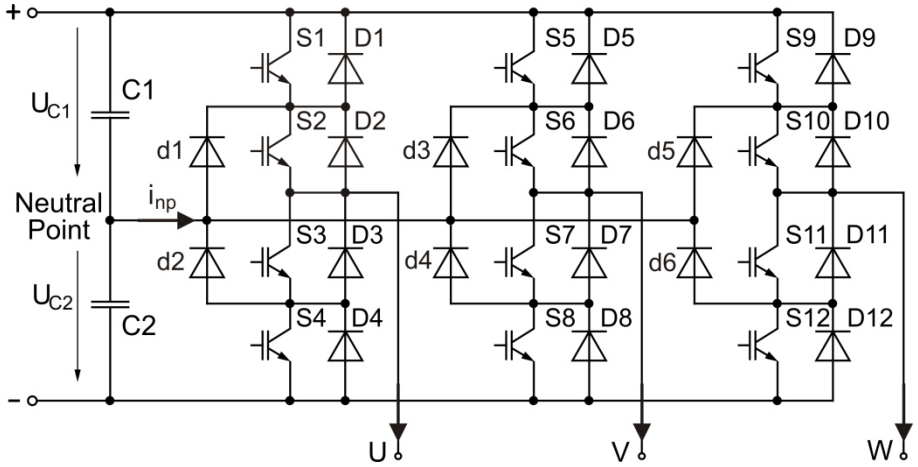
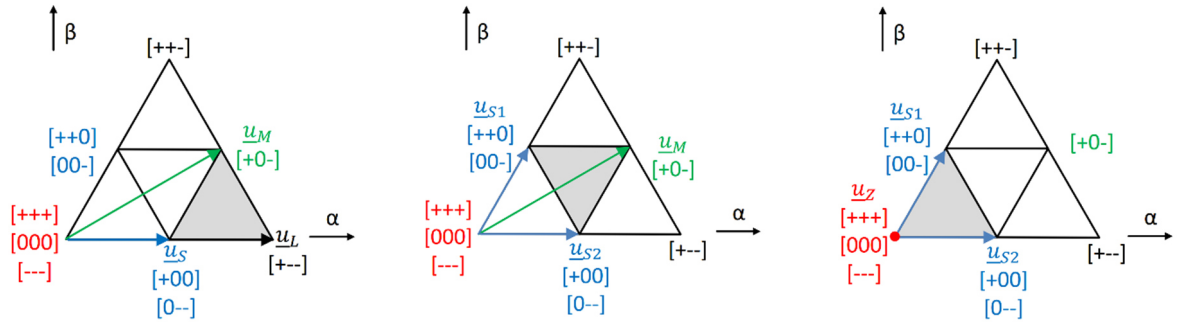


Figure 11: Neutral-point voltage $u_{NP} = U_{C1} - U_{C2}$

2.5.1 Impact of redundancies of short voltage vectors on neutral-point current

Due to symmetry of the space-vector diagram of the 3L-NPC-VSI, it is sufficient to analyze the impact of the redundancies on the neutral-point current i_{NP} only for the sector $0 \leq \theta \leq 60°$ of the space-vector diagram as shown in Figure 12.

It is well known, that the redundant states of short voltage space vectors in a 3L-NPC VSI are pairs, e.g. the $\underline{u}_{S1}$ has two switching states $[+ + 0]$ and $[00-]$ (s. Figure 12). The switching state $[+ + 0]$ connects phase W of the inverter to the neutral point and affects the neutral-point voltage with $i_{NP} = i_W$. In contrast, the switching state $[00-]$ clamps phases U and V of the inverter to the neutral point and $i_{NP} = i_U + i_V = -i_W$. The sign of i_W can be positive or negative depending on the load conditions. In the present work, the *non-inverse redundant states* refer to those ones connecting one phase of inverter to the neutral point, e.g. state $[+ + 0]$ with $i_{NP} = i_W$, while the *inverse redundant states* connect two phases of the inverter to the neutral-point voltage, e.g. $[00-]$ with $i_{NP} = i_U + i_V = -i_W$.



(a) Outer triangle (b) Middle triangle (c) Inner triangle

Figure 12: Effect of long (depicted as black)-, medium (depicted as green)-, short (depicted blue)- and zero (depicted as red) voltage space vectors on the neutral-point current i_{NP}

For the further analysis of the impact of the redundancies on the current flowing into the neutral point, the short space vector e.g. $\underline{u}_{S1}$ depicted in Figure 12 (b) is considered and it is assumed that in a given switching sequence it has the total duty cycle d_{S1}. Moreover, it is assumed that the duty cycle d_{S1} is divided into a sub-duty-cycle of $d_{S1,inverse}$ for the state $[00-]$ and $d_{S1,non-inverse}$ for $[+ + 0]$ that satisfy the conditions

$$\begin{cases} d_{S1,inverse} = \xi \cdot d_{S1} \\ d_{S1,non-inverse} = (1-\xi) \cdot d_{S1} \\ d_{S,non-inverse} + d_{S,inverse} = d_S \\ 0 \leq \xi, \qquad d_{S1} \leq 1. \end{cases} \tag{25}$$

If one of the redundant switching states is not used in the switching sequence, it has consequently a sub-duty-cycle of 0. The *average neutral-point current* $\bar{i}_{NP}$ over the switching period T_S can be simply calculated as:

$$\bar{i}_{NP} = \left(d_{S1,non-inverse} - d_{S1,inverse}\right) \cdot i_W = (1 - 2 \cdot \xi) \cdot d_{S1} \cdot i_W. \tag{26}$$

Obviously, the neutral-point current caused by the short voltage space vector can be controlled by adjusting the weighting factor ξ. If $\xi > 0.5$ the on-time of $[00-]$ becomes longer, and it holds $sign(\bar{i}_{NP}) = -sign(i_W)$. If $\xi < 0.5$, it results in

$sign(\bar{i}_{NP}) = sign(i_W)$. If $\xi = 0.5$, $\bar{i}_{NP} = 0$, without impact on the current of the neutral.

Now based on this, the total neutral-point current will be analyzed in relation to the location of the reference-voltage space vector in one of three triangles: outer, middle and inner triangle as they are depicted in Figure 12.

2.5.1.1 i_{NP} in case of a reference-voltage space vector is located in the outer triangle

The voltage space vectors at the vertices of the shaded triangle in Figure 12 (a) are one short vector $\underline{u}_S$ $[+00]/[0--]$, one medium vector $\underline{u}_M$ $[+0-]$ and one long vector $\underline{u}_L$ $[+--]$. The duty cycles for $\underline{u}_S$, $\underline{u}_M$ and $\underline{u}_L$ are d_S, d_M and d_L respectively and $d_s + d_M + d_L = 1$. The average total neutral-point current is calculated from (26) as:

$$\bar{i}_{NP} = d_M \cdot i_V + \left(d_{S,non-inverse} - d_{S,inverse}\right) i_U. \tag{27}$$

The term $d_M \cdot i_V$ refers to a *non-controllable* component that depends on the output current i_V and on the duty cycle d_M of the medium voltage space vector [40]. The term $(d_{S,non-inverse} - d_{S,inverse}) i_U$ refers to the *controllable* component as explained above.

An increase of the modulation index of the inverter demands switching sequences, in which the duty cycle d_M becomes larger, while the $d_S = d_{S,non-inverse} + d_{S,inverse}$ decreases. This results in a reduction of the control autonomy of the neutral-point voltage, because the effect of the *uncontrollable* component e.g. $d_M \cdot i_V$ becomes harder to be compensated by the *controllable* component e.g. $(d_{S,non-inverse} - d_{S,inverse}) i_U$.

2.5.1.2 i_{NP} in case of a reference-voltage space vector located in the middle triangle

The voltage space vectors at the vertices of the shaded triangle in Figure 12 (b) are of two short vectors $\underline{u}_{S1}$ $[++0]/[00-]$, $\underline{u}_{S2}$ $[+00]/[0--]$ and one medium vector $\underline{u}_M$

$[+0-]$ with the duty cycles d_{S1}, d_{S2} and d_M , respectively, and $d_{S1} + d_{S2} + d_M = 1$. The average neutral-point current is again is calculated from (26) as:

$$\bar{i}_{NP} = d_M \cdot i_V + \left(d_{S1,non-inverse} - d_{S1,inverse}\right) \cdot i_W + \left(d_{S2,non-inverse} - d_{S2,inverse}\right) \cdot i_U. \tag{28}$$

The situation described by (28) is more favorable for the control of the neutral-point current than the case in (27), since two short voltage space vectors are available for the compensation of the influence of the medium voltage space vectors on the neutral-point current.

The outer and middle triangles correspond to the **range of high modulation index**, in which the three nearest-voltage space vectors can be redundant as well as non-redundant. The use of the medium voltage in this modulation index range is unavoidable, therefore the ripple of the neutral-point voltage cannot be completely suppressed, especially in the range of higher modulation index and small power factor $|cos\varphi_P|$ the quality of the control of the neutral-point voltage becomes poor [40].

2.5.1.3 i_{NP} in case of a reference voltage space vector located in the inner triangle

The voltage space vectors at the vertices of the shaded triangle in Figure 12 (c) are two short vectors $\underline{u}_{S1}$ $[++0]/[00-]$, $\underline{u}_{S2}$ $[+00]/[0--]$ and three zero vectors $\underline{u}_Z$ $[---]/[000]/[+++]$ with the duty cycles d_{S1}, d_{S2} and d_Z respectively and $d_{S1} + d_{S2} + d_Z = 1$. Here, the state $[000]$ has no impact on the neutral-point voltage voltage, since $i_{NP} = i_U + i_V + i_W = 0$. The average neutral-point current is given as:

$$\bar{i}_{NP} = (d_{S1,non-inverse} - d_{S1,inverse}) i_W + (d_{S2,non-inverse} - d_{S2,inverse}) i_U. \tag{29}$$

The inner triangles correspond to the **range of low modulation index** of the inverter, which is the most advantageous for the control of the neutral-point voltage. The voltage space vectors at the vertices are only redundant ones, allowing full control of the

neutral-point voltage, thus the ripple of the neutral-point voltage can be suppressed for any value of power factor in this modulation index range.

2.5.2 Control of neutral-point voltage

Due to the current flowing into the neutral-point voltage the voltage distribution on the capacities of the DC link is disturbed. The influence of the switching patterns on the current i_{NP} of the neutral point was explained above and leads to the relationships (27) to (29).

The variations of the i_{NP} produce a change of the neutral-point voltage $u_{NP} = U_{C1} - U_{C2}$ (see Figure 11) according to:

$$(C_1 + C_2)\frac{d}{dt}u_{NP} = i_{NP}, \tag{30}$$

that has to be controlled in order to avoid an imbalance of the capacitor voltages of the DC link.

Two control targets for the neutral-point voltage are reported in the literature:

- The reduction of the neutral-point voltage imbalance due to non-ideal components or distortion from the load side as discussed in [41].
- The elimination of the neutral-point voltage ripple in the high modulation index range as presented in [43]−[46].

Although in the literature the control of the neutral-point voltage is often explained for CB-PWM or for SV-PWM, the equivalence of both methods for this purpose is widely accepted, since the difference among redundant states of a same voltage space vector is in fact the common-mode voltage (zero-sequence voltage). Therefore, the control of neutral-point voltage by using CB-PWM is mostly based on the manipulation of the zero-sequence voltage, while the control methods for SV-PWM are realized by adjusting the use of redundant states of the short voltage space vectors.

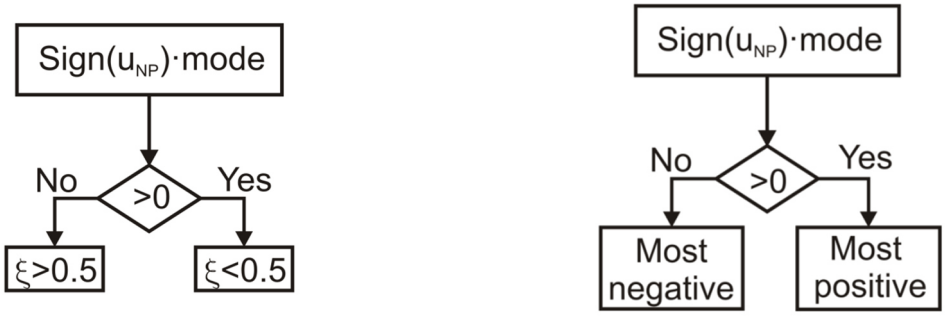
Regarding the control methods for the neutral-point voltage, three approaches are well-known in the literature [40]:

- **Passive control**: the on-times of inverse and non-inverse switching states are adjusted in such way, that an average neutral-point current $i_{NP,avarage} = 0$ is achieved. These methods work ideally only in the steady state for perfect conditions of operation like balanced load, ideal components, etc., that are unlikely to happen in practice.
- **Nonlinear two- or three-step control**: this is simple and commonly used for the closed-loop control of the neutral-point voltage. It requires the knowledge of the sign of the neutral-point voltage ripple and the direction of power flow. There are several different forms of implementation. It can be used with a hysteresis characteristic, but the dynamics of the plant even allows a simple state control without hysteresis.

  A simple scheme of the implementation for SV-PWM is shown in Figure 13, in which the quantity *mode* has two values of 1 or −1, depending on the mode of operation of the converter: motor, i.e. inverter, or regenerative, i.e. rectifier operation, respectively. In case of C-PWM technique, the control is achieved by adjusting the weighting factor ξ as defined in (21) as shown in Figure 13 (a). The values of ξ (larger or less than 0.5) is chosen empirically.

  In case of D-PWM the control scheme is similar, based on the appropriate choice of the switching sequence of the switching matrix. As explained in 2.4.2, the switching sequences have a different impact on the common-mode voltage and the appropriate choice is carried out as shown in the Figure 13 (b).
- **PI based control:** the sub-duty-cycles of the redundant switching states (in case of SV-PWM) or the amplitude of the zero-sequence voltage (in case of CB-PWM) can be also adjusted by using a linear PI controller [27][29]. These control methods may require the measurement of the neutral-point voltage ripple and the magnitude of the phase currents. In [29] a model for the relationship between the neutral-point

current i_{NP} and the required magnitude of the common-mode voltage u_{CMV} to be injected to the reference signals is presented. Furthermore, the non-linear relationship is linearized and used for the design of the PI-control scheme to generate a proper zero-sequence. A method for an enhancement of the neutral-point voltage control quality is proposed in [27].



(a) Choice of proper weighting factor ξ by C-PWM technique

(b) Choice of proper switching sequence by D-PWM technique

Figure 13: Optimization of switching sequence for the reduction of the neutral-point voltage imbalance

In the present work, a nonlinear two-step control without hysteresis is used due to the simplicity of the implementation and the robustness for both C-PWM and D-PWM techniques and has no impact on the core topic of the investigation. The three-step control as proposed in [42] was also examined, but it was discarded because it leads to an increase of the number of switching actions and thus of the losses for small values of the error signal.

2.6 Control schemes for induction machines

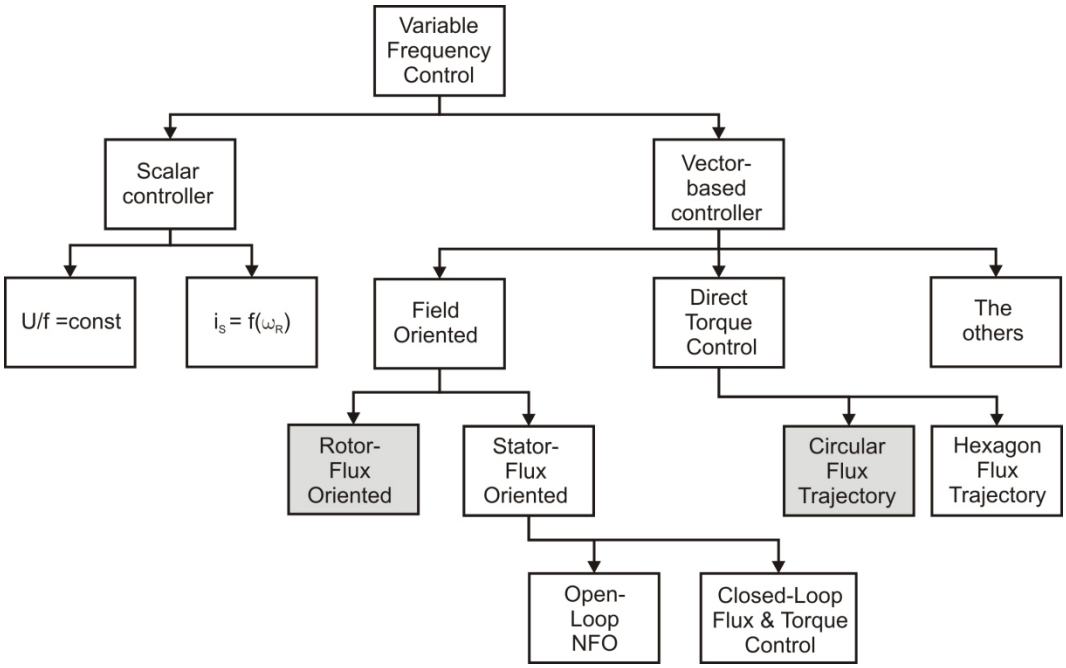


Figure 14: Classification of IM control methods [23], the shaded boxes refer to methods implemented in the present work

In the present work, the 3L-NPC VSI connected to an induction machine is used as the laboratory set-up to verify the ALE control strategy. Thus, a brief introduction of the control of induction machine is presented in the following. As it can be seen in Figure 14, the control methods can be classified into two groups:

- **Scalar control schemes:** these methods are based on the relationships of magnitude and frequency of e.g. voltage, currents, etc. in the steady state. They are mostly applied in low-cost drives and feature simple implementation and robustness at the cost of poor dynamic.
- **Vector-based control schemes:** Not only the magnitude and the frequency, but also the instantaneous angular positions (phases) of the voltage, current and flux space vectors are taken into consideration. As a result, the vector-based control method offers excellent dynamics and better efficiency in the whole operational range. Thanks to the widespread use of microcontrollers and power electronics, the

adjustable-speed drive systems became more and more competitive and have replaced the fixed-speed drives in many industrial applications.

An adjustable-speed drive consists typically of an AC machine and a voltage source inverter (VSI). Depending on the control of inverter, the vector-based control methods can be further divided into two sub-groups: indirect and direct control. The direct methods employ hysteresis controllers to select the proper switching pattern to control inverter. The switching-table-based Direct Torque Control (DTC) is one of the most well-known methods. These methods feature excellent dynamic, simple structure, robustness, etc. However, they are subject to variable switching frequency that is not always of advantage in drives. In case of the indirect control methods, the inverter is operated at fixed switching frequency, where the control structures comprise an inner control loops and a modulator, which undertakes the task of generating the switching pattern for the control of the inverter. Field-Oriented Control (FOC) is one of the widely used variants.

The PWM with ALE will be examined with both control methods: FOC (*with modulator*) and switching-table based DTC (*without modulator*). The used control methods for the present work are shaded in Figure 14.

2.6.1 Rotor-flux-based field-oriented control

For the rotor-flux-orientated control of the induction machine, an orthogonal d,q-rotor-flux-oriented coordinate system is assumed, in which the d-axis is aligned with the rotor- flux space vector $\underline{\psi}'_R$. The controlled variables of the induction machine are transformed into this coordinate system and two fundamental equations for the FOC can be obtained as:

$$\frac{d}{dt}\left|\underline{\psi}_R'\right| + \frac{1}{\tau_R'} \cdot \left|\underline{\psi}_R'\right| = \frac{L_{S,h}}{\tau_R'} i_{S,d} \,. \tag{31}$$

$$M_i = k_f \left|\underline{\psi}_R'\right| i_{S,q} \,. \tag{32}$$

Where $\tau_R' = \frac{L_R'}{R_R'}$ is the time constant of the rotor and k_f is a constant factor. The amplitude of the rotor-flux linkage $\left|\underline{\psi}_R'\right|$ can be manipulated by using the d-component of stator current $i_{S,d}$ due to the relationship (31). $i_{S,d}$ is consequently named flux-producing component of the stator-current space vector $\underline{i}_{S,dq} = i_{S,d} + j \cdot i_{S,q}$ in the d, q-rotor-flux-oriented coordinate system. If the component $i_{S,d}$ is kept constant, then the amplitude of rotor flux $\left|\underline{\psi}_R'\right|$ is unchanged in the steady state. Yet the electromagnetic torque M_i in (32) is directly proportional to the q-component of stator current $i_{S,q}$, hence this is called torque-producing component of $\underline{i}_{S,dq}$. The induction machine operated with this control scheme behaves like a separately excited DC machine, since the control of torque and flux is decoupled.

The magnitude of the rotor-flux linkage $\left|\underline{\psi}_R'\right|$ and its instantaneous position $\varphi_{\psi,R}$ are required for the FOC control scheme. The direct measurement of these is cumbersome, thus the unknown variables are estimated by using a flux model. Two simple methods are used to estimate the $\left|\underline{\psi}_R'\right|$ rotor-flux space vector [26]:

Current-based model: the magnitude of the rotor flux can be obtained with (31) and the instantaneous position is calculated as:

$$\varphi_{\psi,R} = \int \omega_R \, dt + \int \frac{L_{S,h} \cdot i_{S,q}}{\psi_R' \cdot \tau_R'} dt \,, \tag{33}$$

ω_R denotes the electrical angular frequency of the rotor. The current-based model features simple implementation and is applicable for the whole speed range. However, the main drawbacks of this method are the temperature sensitivity due to the strong tem-

perature dependence of the rotor time constant $\tau_R^{'}$ and the need of an expensive sensor for measuring the rotor speed.

Voltage-based model: In this case the α, β-stator-oriented coordinate system is employed, where the α-axis is aligned with the axis of phase U of the machine. The equation in (5) can be rewritten in the α, β-stator-oriented coordinate system as:

$$\underline{\psi}_{S,\alpha\beta} = \int (\underline{u}_{S,\alpha\beta} - R_S \cdot \underline{i}_{S,\alpha\beta}) dt. \tag{34}$$

Then the rotor-flux space vector can be obtained as:

$$\underline{\psi}'_{R,\alpha\beta} = \frac{\sigma}{\sigma - 1} \cdot L_h \cdot \underline{i}_{S,\alpha\beta} + (1 + \sigma_R) \cdot \underline{\psi}_{S,\alpha\beta}\ , \tag{35}$$

where the leakage factors are given in (9). The magnitude and the phase angle of $\underline{\psi}^{'}_{R,\alpha\beta}$ are obtained by changing form Cartesian to polar coordinate system as $\left|\underline{\psi}'_R\right| = \sqrt{(\psi'_{R,\alpha})^2 + (\psi'_{R,\beta})^2}$ and $\varphi_{\psi,R} = \text{atan}(\frac{\psi'_{R,\beta}}{\psi'_{R,\alpha}})$ for the case $\psi'_{R,\alpha} \neq 0$.

By using the voltage model, the knowledge of the rotor position is not required, hence the measurement of rotor speed is obviated. The temperature dependency of the stator resistance R_S in (34) can be easily compensated. However, this method does not work well in the range of low frequency. Therefore, the current and voltage model can be combined to provide a proper operation for the whole speed range [26].

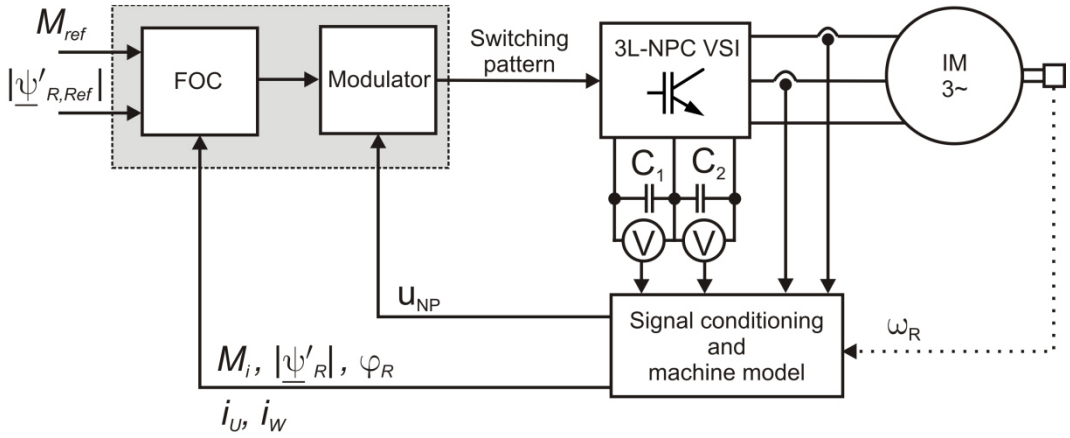


Figure 15: FOC scheme for 3L-NPC VSI

Figure 15 shows the FOC scheme for a 3L-NPC VSI fed induction machine, where the reference values of torque M_{ref} and rotor flux $\left|\underline{\psi}'_{R,ref}\right|$ are compared with actual values M_i and $\left|\underline{\psi}'_R\right|$ by the controllers to generate the reference currents. The reference currents are subsequently handled by the current controllers to generate the reference phase voltages. The reference voltage is synthesized by using the modulator, which generates the switching pattern to control the switches of inverter. In a 3L-NPC VSI, the neutral-point voltage ripple is also taken into consideration by generating the switching patterns.

The Active Lifetime Extension (ALE) to be developed in the following modifies the switching patterns aiming at an active relocation of the losses among the switching devices of the inverter, but without any kind of modifications in the basic field-oriented control.

2.6.2 Direct Torque Control

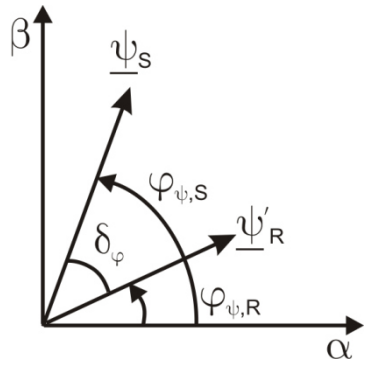


Figure 16: The fluxes in α, β-stator oriented coordinate system

In a basic analysis of Direct Torque Control [27], the stator resistance can be assumed to be small and is neglected. Thus, the equation (5) can be rewritten in the α, β-stator-oriented coordinate system as:

$$\frac{d}{dt}\underline{\psi}_{S,\alpha\beta} \approx \underline{u}_{S,\alpha\beta}. \tag{36}$$

The equation can be further approximated for a small time increment of Δt:

$$\Delta\underline{\psi}_{S,\alpha\beta} \approx \underline{u}_{S,\alpha\beta} \cdot \Delta t. \tag{37}$$

The electromagnetic torque is expressed as a function of stator and rotor flux:

$$M_i = \frac{3}{2} \cdot p \cdot \frac{1-\sigma}{\sigma \cdot L_{S,h}} \cdot \left|\underline{\psi}'_{R,\alpha\beta}\right| \cdot \left|\underline{\psi}_{S,\alpha\beta}\right| \cdot sin\delta_\varphi \,, \tag{38}$$

p is the number of pole pairs of the machine and the angle δ_φ refers to load angle as illustrated in Figure 16. Due to the large value of the rotor time constant, for a short time period Δt the rotor-flux space vector $\underline{\psi}'_{R,\alpha\beta}$ can be considered as to be virtually fixed to the rotor. In contrast, the stator flux $\underline{\psi}_{S,\alpha\beta}$ can be rapidly changed by the applied stator voltages according to (37). The induction machine is supplied with a voltage source inverter, which generates only a finite number of output-voltage space vectors. The selection of the proper output-voltage space vector follows the simple control

rule: If an increase of torque is required, the voltage space vector that causes the movement of $\underline{\psi}_{S,\alpha\beta}$ away from $\underline{\psi}'_{R,\alpha\beta}$ is chosen to increase the load angle δ_φ in (38). Conversely, if a decrease of the torque is needed, the voltage space vector causing the reduction of the load angle δ_φ is chosen accordingly. The control of the induction machine under a DTC scheme does not require either modulator or coordinate transformation and current controllers are obviated. Thus, this control method is very attractive because of its simplicity and additionally higher dynamic.

The Figure 17 shows the switching-table-based DTC scheme for an induction machine fed by a 3L-NPC VSI. The reference values of torque M_{ref} and stator-flux magnitude $\left|\underline{\psi}_{S,\alpha\beta,ref}\right|$ are compared with the actual values M_i and $\left|\underline{\psi}_{S,\alpha\beta}\right|$, delivered by the machine model (observer). The control errors are fed to hysteresis controllers to maintain the controlled variables staying within the pre-defined bands. The switching patterns are generated by employing a look-up table. The estimation of stator-flux space vector $\underline{\psi}_{S,\alpha\beta}$ and electromagnetic M_i in the machine model is realized by using the equations (34) and (38). The choice of the proper switching state is based on the outputs of hysteresis controllers, the neutral-point-voltage deviation and the location of stator-flux space vector. To apply the ALE strategy to a DTC scheme, the redundant switching states stressing the weak switches have to be excluded from switching table, and the other redundant states have to be used instead.

Prior to the experimental verification, the impact of the control methods with ALE on the loss production of the switches of 3L-NPC VSI has to be examined by means of simulation. Thus, the method for estimation of the losses of switching device will be introduced in the following.

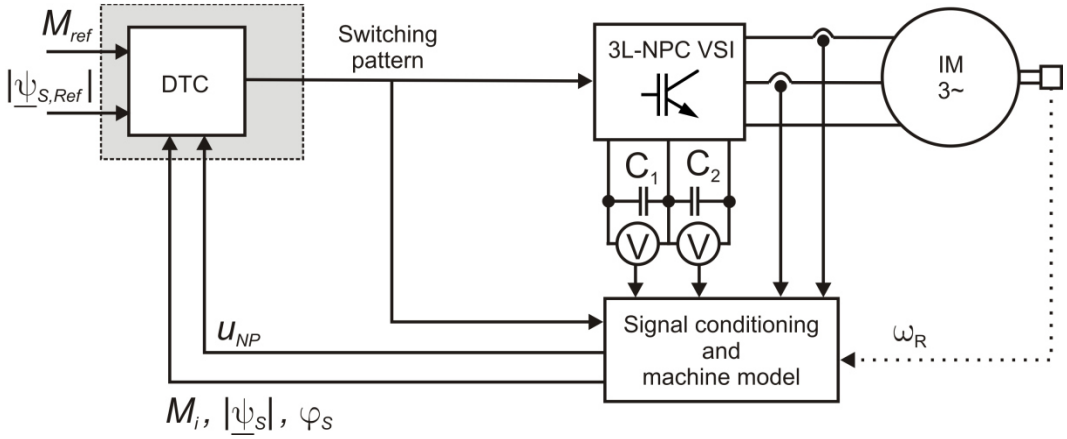


Figure 17: DTC scheme for 3L-NPC VSI using switching table

2.7 Estimation of losses in semiconductors devices

The thermal losses produced by a semiconductor device, e.g. IGBT, comprise two components: switching and conduction losses. The conduction losses of IGBTs are calculated as:

$$P_{Conduction} = u_{CE}(i_C) \cdot i_C = \left(u_{CE,0} + i_C \cdot r_{CE}\right) \cdot i_C. \tag{39}$$

The term $u_{CE}(i_C)$ refers to the on-state voltage drop across the IGBT during the conduction state and is considered as a function of the current i_C. The voltage $u_{CE}(i_C)$ consists of two terms: $u_{CE,0}$ is the offset voltage, $i_C \cdot r_{CE}$ describes the linearized relationship between voltage drop and conduction current. The term i_C denotes the instantaneous collector current flowing through the switch. The offset voltage $u_{CE,0}$ and the differential resistance r_{CE} are extracted directly from the on-state characteristics curve in the data sheet of the switch.

The method for the estimation of the switching losses by using a pulse counter is proposed in [28], where it takes into account each individual turn-on and turn-off action of the switch. The energy associated to the switching losses of an IGBT for each switching action is specified as:

$$E_{Switch} = E_{Switch,0} \cdot \frac{\frac{U_{DC}}{2}}{U_{DC,0}} \cdot \frac{i_C}{I_{C,0}}. \tag{40}$$

The base switching energy dissipation $E_{Switch,0}$ is a constant value and is obtained from the data sheet for a given test condition with $U_{DC,0}$ and $I_{C,0}$. Obviously, every IGBT of the 3L-NPC inverter must withstand, at most, a maximum commutation voltage of $U_{DC}/2$. The energy E_{Switch} stands for either turn-on or for turn-off loss energy. The average switching power losses can be calculated by using the sample frequency of the control scheme as:

$$P_{Switch} = f_{Sample} \cdot E_{Switch}, \tag{41}$$

finally the average overall losses are computed as:

$$P_{Loss} = P_{Conduction} + P_{Switch,on} + P_{Switch,off}. \tag{42}$$

In a similar manner, the estimation of the conduction losses and recovery losses of a diode can be carried out with (39)-(42). Since the diodes are not controllable, the turn-off action of the diode is calculated in the simulation in a model that takes into account the zero crossing and the slope of current through the diode.

The simulation of the distribution of losses among the switches in a 3L-NPC VSI comprises two steps: at first, the simulation of the induction machine fed by the 3L-NPC VSI and controlled by a field-oriented or a DTC scheme is carried out for obtaining the current and the switching pattern of each semiconductor device. In a second step, this information is used as input for the thermal model to calculate the losses of each switch.

3 Modification of PWM aiming at a reduction of losses

It is well known that the operation of an inverter using C-PWM provides better harmonic performance but at the cost of higher switching losses as compared with the D-PWM technique, which is applied with the same sampling frequency [19]. In practice, the C-PWM technique is widely used to generate the switching patterns for the control of the inverter.

As already explained the objective of this investigation is the development of a modified switching strategy that leads to a reduction of losses in a particular switch or group of switches.

If thermal overload is detected in one switching device or in one switching group, the first step toward a reduction of losses shall be to switch from the continuous PWM scheme to the discontinuous PWM scheme (with same carrier frequency). Therefore PWM with the ALE proposed in this work will be operated in a two-step mode. In the first step, the switching sequence is generated with D-PWM instead of C-PWM. Consequently, the control of the neutral-point voltage imbalance has to be adapted and the switching sequence accordingly optimized. Thanks to the use of D-PWM, the reduction of losses can be achieved with a minimum impact on the system performance, i.e. on the quality or on THD of the output currents. If this first action is still not sufficient to keep the stressed device or the affected group of switches under the allowed thermal limit, a second step is necessary: the switching sequence is optimized to reduce the losses of the affected devices. For this purpose an enhanced D-PWM technique will be developed that considers two control targets: the balancing of the neutral-point voltage and the transfer of the losses to other switches or groups of switches. This new PWM technique will be referred as PWM with Active Lifetime Extension (ALE), because as explained in the introduction that aims at a reduction of the losses in order to extend

the lifetime of a switch or a group of switching devices that work under adverse thermal conditions.

In following, the conventional D-PWM is used as *reference and basis of comparison for the evaluation of the results obtained by PWM with ALE.* In the implementation of the conventional D-PWM either in simulation or in the experiments, the switching sequence is optimized only regarding the reduction of the imbalance of the neutral-point voltage. If D-PWM is modified aiming at a reduction of the losses in a switch, the modulation technique is referred as “PWM with ALE” or simply ALE.

During the operation of PWM with ALE, the stability of the neutral-point voltage must be ensured for all the time. Therefore, the developed PWM with ALE has to be combined with the control of the voltage of the neutral-point voltage. In the present case, the balancing of the neutral-point voltage is achieved by means of a two-step control as explained in 2.5.2. In addition to this, a superimposed hysteresis control is used for the operation of the PWM with ALE together with the imbalance control. As long as the voltage of the neutral-point voltage is within the tolerance band of this superimposed hysteresis control, the PWM with ALE can be applied, if the magnitude of the neutral-point voltage ripple becomes larger than the predefined threshold band, the PWM with ALE is deactivated and the control returns to the conventional D-PWM. The width of the hysteresis has to be chosen in a suitable way. If it is too large, then the harmonic distortion on the output currents of the inverter increases due to the higher ripple on the neutral-point voltage. However, if the hysteresis band is set too narrow, the switching between PWM with ALE and D-PWM causes higher switching losses and reduces the system efficiency. Hence, the choice of the proper value of the hysteresis band requires also a tradeoff.

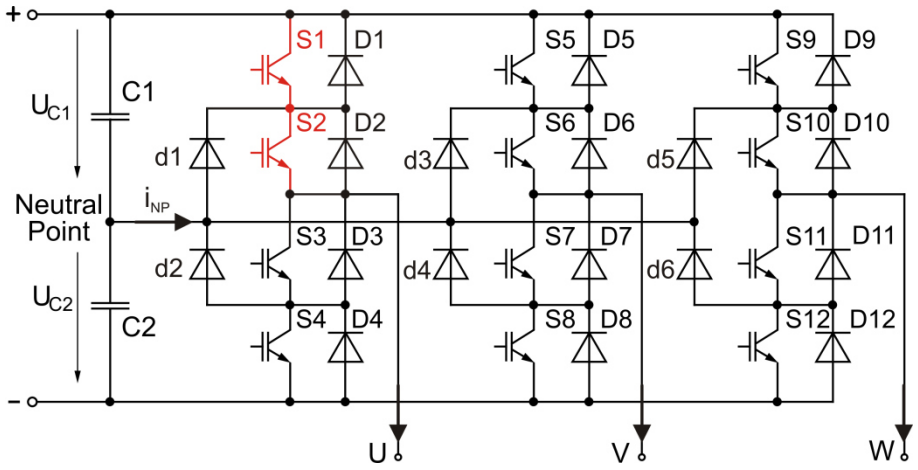


Figure 18: 3L-NPC Inverter ; a thermal overload of the upper leg of phase U (in red) is assumed

Without loss of generality, in the following explanations of the PWM with ALE it is assumed that the upper leg of phase U, depicted in red in Figure 18, is suffering from thermal overload and ALE is applied to reduce its losses. Depending on the range of modulation index of the inverter a different approach for redistribution of the losses based on redundancies is necessary, therefore the analysis discerns ALE in the range of low and of high modulation index.

3.1 Modification of PWM in range of low modulation index

In following, the modulation index m is defined as:

$$m = \frac{U_{LL}}{U_{DC}/\sqrt{2}}. \tag{43}$$

The term U_{LL} refers to the effective value (rms) of the fundamental line-to-line voltages to be synthesized by the inverter and U_{DC} is the value of the DC-link voltage of the 3L-NPC VSI; it ranges from 0 to 1, neglecting the influence of inverter minimum on/off time.

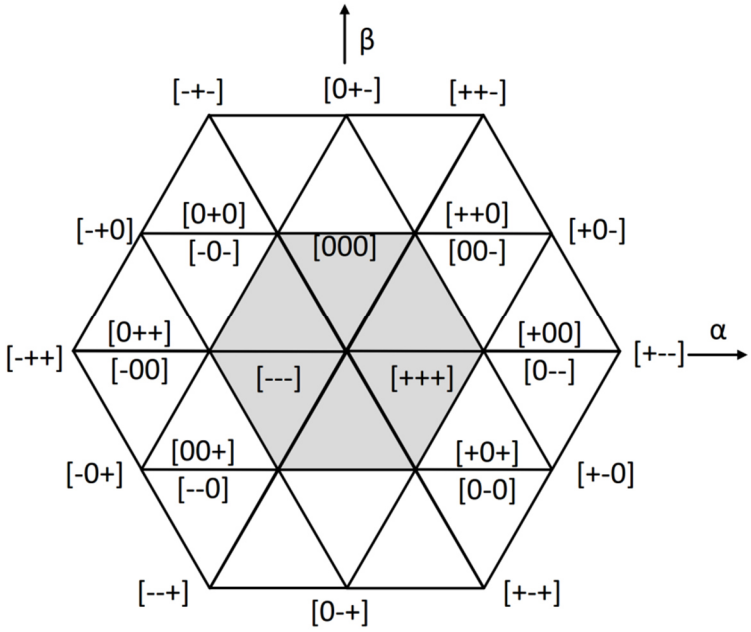


Figure 19: Definition of ranges of modulation index in case of 3-L inverter

The range of low modulation index is depicted as shaded region in the space-vector diagram of the 3L-NPC-VSI in Figure 19; the modulation index is $0 \leq m \leq 0.5$. The range is characterized by consisting of only inner triangles (as explained in 2.5.1), where the switching states at the vertices of any triangle are redundant.

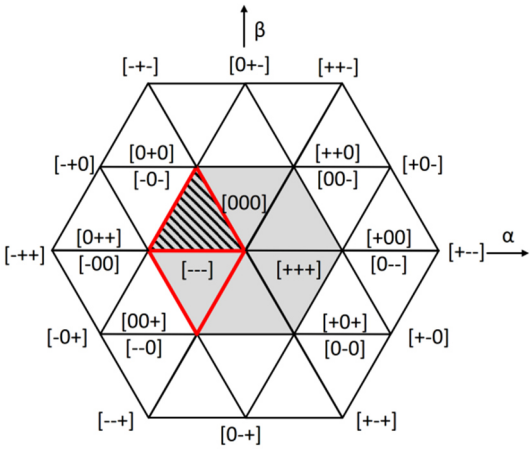
The PWM with ALE developed in this work aims to a reduction of the conduction or switching losses in a single switch or in a group of semiconductor switches. Nevertheless, it is evident that losses have to be distributed to the other semiconductors in the inverter. Therefore, the impact of PWM with ALE on losses of each semiconductor has to be investigated by means of simulations and measurements, as it will be presented in other sections of this work.

ALE is based on the principle that those switching states yielding losses in the affected switch must be avoided and replaced by the redundant states, so that the switch is thermally relieved. Since the number of switching states that can be removed from the switching sequence is associated with the more inner or more outer location of the reference voltage vector on the α, β- complex plane, three different cases for the range of low modulation index are analyzed in the following.

3.1.1 Elimination of one state from switching matrix

In the first case, it is assumed that the reference-voltage space vector lies in the range of low modulation index (shaded in gray) and in one of the triangles with red edges in Figure 20 (a). If the reference voltage space vector is located within the hatched triangle, the corresponding switching states are shown in Figure 20 (b). A similar analysis can be carried out for the other triangle with red edges.

In normal operation with D-PWM, a set of *three adjacent* vectors is taken from the switching matrix to build the switching sequence. There is only one IGBT switching at each state transition. Furthermore, the switching sequence with highest common-mode voltage and the one with lowest common-mode voltage are to be used alternately (see 2.4.2), in order to stabilize the neutral-point voltage of the DC link in the dedicated control loop depicted in Figure 13.



$$\begin{bmatrix} - \\ - \\ - \end{bmatrix} \begin{bmatrix} - \\ 0 \\ - \end{bmatrix} \begin{bmatrix} - \\ 0 \\ 0 \end{bmatrix} \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} \begin{bmatrix} 0 \\ + \\ 0 \end{bmatrix} \begin{bmatrix} 0 \\ + \\ + \end{bmatrix} \begin{bmatrix} + \\ + \\ + \end{bmatrix}$$

(a) The reference-voltage space vector is located inside the hatched triangle

(b) Switching matrix with the states corresponding to the hatched triangle.

Figure 20: Switching state affecting the switches 1 and 2 for a reference voltage vector in the hatched triangle

If PWM with ALE is applied to relieve the upper leg of phase U, the switching state $[+\,+\,+]$ depicted in red in Figure 20 (b), that requires a connection of the upper leg of phase U to the positive DC rail, will be excluded from the calculation and replaced by its redundant states $[000]/[-\,-\,-]$. In this way, the conduction and switching losses of S1 are completely eliminated and those of S2 are reduced.

After the elimination of these states the reference-voltage space vector is synthesized by building a switching sequence with the remaining states.

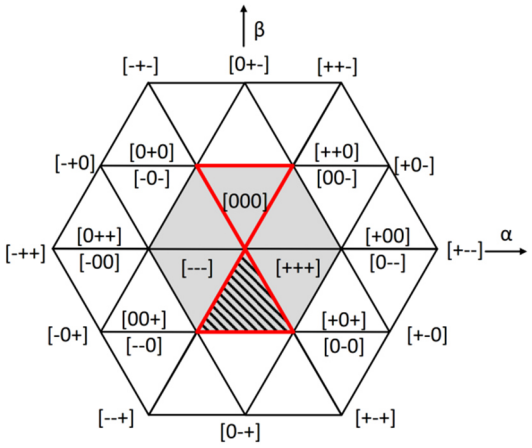
Regarding the impact of ALE on the control of the neutral-point voltage, the switching matrix contains always seven different switching states in the range of low modulation index. Three of them are zero-voltage vectors and the other four are active voltage vectors. After elimination of the undesired switching state, the switching matrix has 6 states. Thus, different switching sequences can be used to synthesize the reference voltage vector and the control of neutral-point voltage is still possible. Therefore, this case is expected to have the smallest impact on the balancing of the neutral-point voltage.

3.1.2 Elimination of two states from switching matrix

In the second case, it is assumed that the reference-voltage space vector lies in one of the triangles highlighted in red in Figure 21 (a). As in the previous case, the analysis is carried out for a reference space vector located in the hatched triangle in Figure 21 (b) and can be applied in a similar manner for the other red highlighted triangle.

As explained above, by avoiding the utilization of switching states depicted in red in Figure 21 (b) that connect the phase U to the upper rail of the DC link, the losses in S1 can be completely reduced and those in S2 partially. Thus$[0\ -\ 0]$ is substituted for $[+\ 0\ +]$, and $[+\ \ +\ \ +]$ replaced by $[0\ 0\ 0]/[-\ -\ -]$.

After this procedure the switching matrix contains five switching states and the balancing of the neutral-point voltage is still possible.



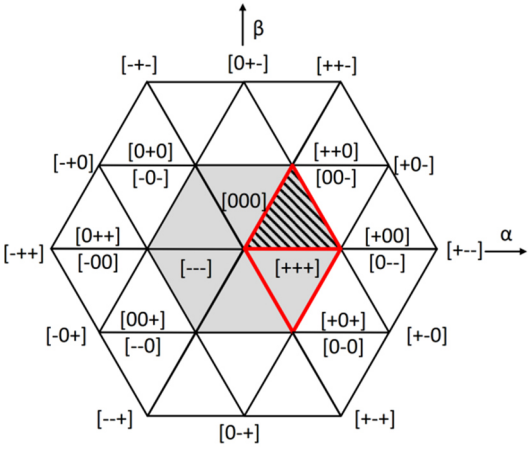
$$\begin{bmatrix} - & - & 0 & 0 & 0 & + & + \\ - & - & - & 0 & 0 & 0 & + \\ - & 0 & 0 & 0 & + & + & + \end{bmatrix}$$

(a) The reference-voltage space vector is located inside the hatched triangle

(b) Switching matrix for the hatched triangle.

Figure 21: Switching states affecting IGBTs 1 and 2 for a reference voltage vector located in the hatched triangle

3.1.3 Elimination of three states from switching matrix



$$\begin{bmatrix} - & 0 & 0 & 0 & + & + & + \\ - & - & 0 & 0 & 0 & + & + \\ - & - & - & 0 & 0 & 0 & + \end{bmatrix}$$

(a) The reference-voltage space vector is located inside the hatched triangle

(b) Switching states of the hatched triangle sorted in a switching matrix.

Figure 22: Switching states affecting IGBTs 1 and 2 (in red) for a reference voltage vector located in the hatched triangle

In the last case to be considered, the reference-voltage space vector lies in one of the red highlighted triangles in Figure 22 (a). The analysis is carried out for a voltage space vector located in the hatched triangle and it can also be extended for the other

red highlighted triangle. The switching states of the hatched triangle are shown in Figure 22 (b).

As in the two previous cases, the strategy of reducing the losses is realized by eliminating the switching states depicted in red in Figure 22 (b) that connect the phase U to the upper rail of the DC link. Thus $[+\ 0\ 0]$ is replaced by$[0\ -\ -]$, state $[+\ +\ 0]$ by $[0\ 0\ -]$, and $[+\ +\ +]$ by $[0\ 0\ 0]/[-\ -\ -]$. By this way, the losses in S1 can be completely omitted and those in S2 partially reduced.

The switching matrix after this procedure has four switching states which still allow the control of the neutral-point voltage. However, this is the most disadvantageous case for the balancing of the neutral-point voltage in the range of low modulation index.

3.2 Modification of PWM in range of high modulation index

PWM with ALE for the range of low modulation index can be realized in a straightforward manner by avoiding the switching states affecting a particular switch, thus the stressed devices do not participate in the modulation. Unfortunately, for the range of high modulation index a complete exclusion of the affected switching devices from the modulation is not possible, as the obtained switching sequence in this range does not only contain *redundant* voltage space vectors, but also *non-redundant* space vectors. Therefore, the optimization of switching sequence has to be considered in a different manner in order to reduce the losses in the stressed switches.

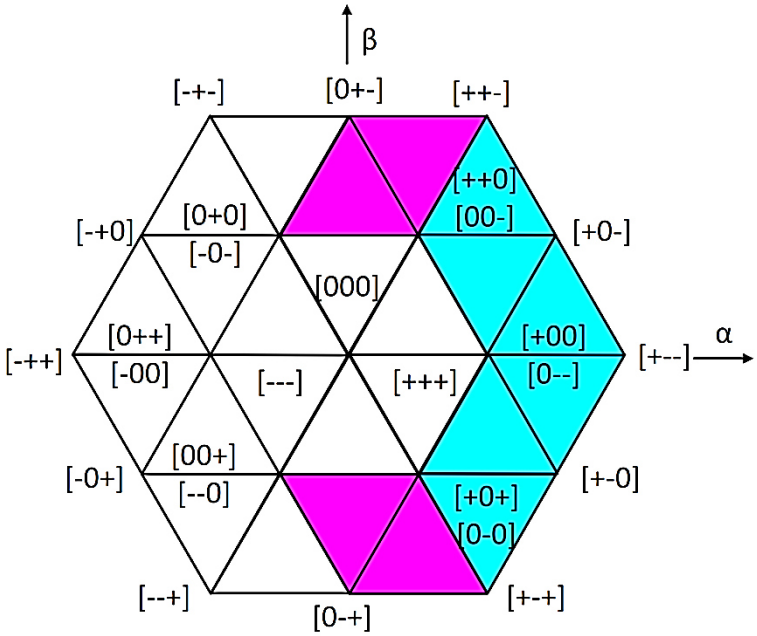


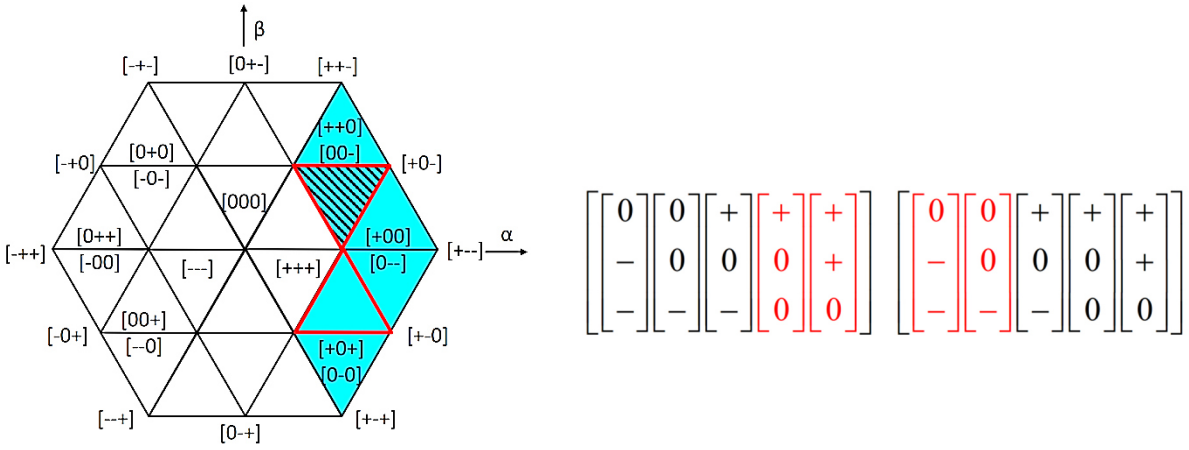
Figure 23: Region for the application of PWM with ALE in the range of high modulation index

For the further explanations, the range of high modulation index is divided into three sub-regions depicted in white, in blue and in magenta as shown in Figure 23. In each of these sectors the impact of the PWM on the losses has to be examined in a different way.

The region in white contains switching states that do not use the switch S1 of the upper leg of phase U. In fact, the sectors in magenta use S1, but the measurements and simulations have shown that is better to exclude them from the PWM with ALE in favor of a better imbalance control. Therefore, if the reference-voltage space vector is located in one of these sectors highlighted in white or magenta, the PWM with ALE is *not active* and the inverter is operated with the conventional D-PWM.

If the reference voltage vector lies in the regions highlighted in blue, a reduction of losses of the upper leg of phase U can be achieved by choosing the appropriate states of the switching matrix. For this purpose, an analysis that depends on the location of the reference-voltage space vector and on the dominant type of losses i.e. switching or conduction losses has to be performed and yields different control strategies.

3.2.1 Sectors with five switching states affecting losses in one phase



(a) The reference-voltage space vector is located in the hatched triangle

$$\begin{bmatrix} 0 \\ - \\ - \end{bmatrix} \begin{bmatrix} 0 \\ 0 \\ - \end{bmatrix} \begin{bmatrix} + \\ 0 \\ - \end{bmatrix} \begin{bmatrix} + \\ 0 \\ 0 \end{bmatrix} \begin{bmatrix} + \\ + \\ 0 \end{bmatrix}$$

(b) Avoiding the states in red reduces the conduction and increase the switching losses in S1 and S2

$$\begin{bmatrix} 0 \\ - \\ - \end{bmatrix} \begin{bmatrix} 0 \\ 0 \\ - \end{bmatrix} \begin{bmatrix} + \\ 0 \\ - \end{bmatrix} \begin{bmatrix} + \\ 0 \\ 0 \end{bmatrix} \begin{bmatrix} + \\ + \\ 0 \end{bmatrix}$$

(c) Avoiding the states in red reduces the switching and increases the conduction losses in S1 and S2

Figure 24: ALE for upper leg of phase U in the range of high modulation index.

In the following, the reference-voltage space vector is located in one of the triangles bordered red in Figure 24 (a). In order to illustrate the different PWM with ALE, it is first assumed that it lies inside the hatched triangle and the corresponding switching matrices are shown in Figure 24 (b) and (c). The same considerations can be made for the other triangle bordered red.

For the selection of the optimum switching sequence with regard to the losses, the type of losses affected by the particular sequence has to be taken into account. As treated in 2.7, the thermal losses consist of switching and of conduction losses. Thus, the redundant states can be utilized for the reduction of either switching losses or conduction losses.

3.2.1.1 PWM aiming at a reduction of conduction losses

Figure 24 (b) shows switching states in red and in black. If the redundant states [+ + 0] and [+00] (short voltage space vectors) are excluded from the modulation sequence

and only the states depicted in black are used, the PWM demands only one switching state out of three in which the upper leg of phase U is connected to the upper rail. Hence, by favoring such switching sequences, the **conduction losses** of the upper leg of phase U i.e. of S1 and S2 are **reduced**.

Of course, the reduction of conduction losses depends on the modulation index, on the load and on the conduction times associated with the pulse pattern. In addition, it implies also an increase of the switching losses of the same semiconductor devices. In fact, the switching state [+0−] should also be excluded to reduce the conduction losses of S1 and S2. Unfortunately, this state is non-redundant and its exclusion reduces the current quality significantly. Such operation is hardly accepted in the field.

3.2.1.2 PWM aiming at a reduction of switching losses

If the switching states depicted in red in Figure 24 (c) are avoided, and the switching states in black are used instead in the switching sequence, the upper leg of phase U remains clamped to the positive DC-rail during the whole modulation period. By favoring this sequence, the switching losses are reduced at the cost of higher conduction losses.

3.2.1.3 Choice of the appropriate approach

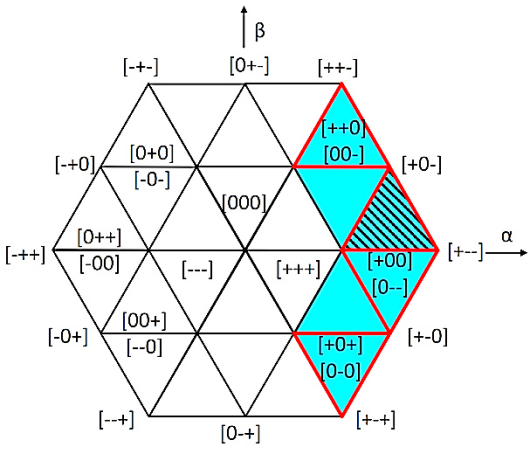
As explained above, the optimization of the switching patterns exhibits concurrent targets and leads therefore to a dilemma, as the reduction of the conduction losses leads to higher switching losses and vice versa. Thus, the consideration of other aspects is mandatory. The operation of the inverter at higher modulation index yields switching sequences, in which the on-time of the short voltage space vectors decreases. The approach based on reduction of conduction losses by taking advantage of redundancies of short voltage space vectors is therefore limited at high values of the modulation index. Conversely, the reduction of the switching losses is independent from the on-time of the short voltage space vectors for the same switching sequences. Furthermore, the switching losses in power semiconductor devices for medium voltage applications are particularly high. Hence, the reduction of switching losses is preferable in this range of high modulation index.

As the simulations and measurements have shown, the proposed method will not always achieve a maximal reduction of the conduction or switching losses for the choice of the appropriate approach, the total losses i.e. conduction and switching losses have thus to be considered.

In all sectors with five switching states affecting the losses in one phase after the application of ALE procedure the resulting switching sequence contains only three states, as result, the control of the neutral-point voltage is not possible.

3.2.2 Sectors with four switching states affecting losses in one phase

Now the case of a space vector located in one of the outer triangles that are highlighted in blue and bordered red in Figure 25 (a) is considered. Again for the explanations the reference-voltage space vector is assumed to lie inside the hatched triangle. The corresponding switching matrices that contain four different states shown in Figure 25 (b) and (c). The same analysis can be carried out for a reference-voltage space vector located in the other red-bordered triangles.



$$\begin{bmatrix} 0 \\ - \\ - \end{bmatrix} \begin{bmatrix} + \\ - \\ - \end{bmatrix} \begin{bmatrix} + \\ 0 \\ - \end{bmatrix} \begin{bmatrix} + \\ 0 \\ 0 \end{bmatrix} \qquad \begin{bmatrix} 0 \\ - \\ - \end{bmatrix} \begin{bmatrix} + \\ - \\ - \end{bmatrix} \begin{bmatrix} + \\ 0 \\ - \end{bmatrix} \begin{bmatrix} + \\ 0 \\ 0 \end{bmatrix}$$

(a) The reference-voltage space vector is located in the hatched triangle

(b) Avoiding the states in red reduces the conduction losses and increase the switching losses in S1 and S2

(c) Avoiding the states in red reduces the switching losses and increases the conduction losses in S1 S2

Figure 25: ALE for upper leg of phase U in the range of high modulation index.

As in the previous cases, the aim of the PWM with ALE is the reduction of losses in the upper leg of phase U by using appropriate switching sequences.

3.2.2.1 PWM aiming at a reduction of conduction losses

In order to reduce the conduction losses of the upper leg of phase U and relieve S1 and S2, the switching state $[+00]$ connecting phase U to the positive DC rail (depicted in red in Figure 25 (b)) has to be excluded from the calculation and replaced by $[0--]$. This happens at the expense of higher switching losses.

3.2.2.2 PWM aiming at reduction of switching losses

By favoring a sequence in which the state $[0--]$ (in red in Figure 25 (c)) is not included and replaced by$[+\ 0\ 0]$, the switching losses are reduced at the cost of higher conduction losses.

3.2.2.3 Choice of the appropriate approach

As in the previous cases and due to the same reasons as explained in 3.2.1.3, the reduction of switching losses is preferable in the range of high modulation index.

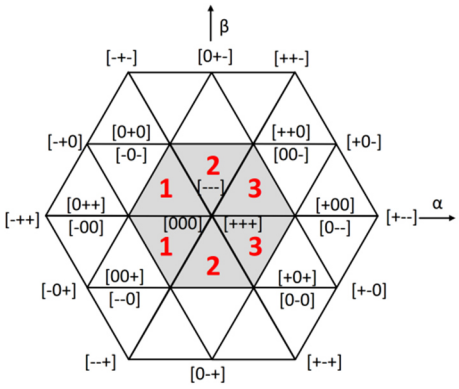
It is evident that after application of ALE only three switching states are left in the switching matrix and the control of the neutral-point voltage is not possible anymore. Therefore, if the reference voltage vector enters the blue region, regardless of the location of the reference voltage vector the balancing of the neutral-point voltage is suspended.

3.3 Application of PWM with ALE to the other legs of the inverter

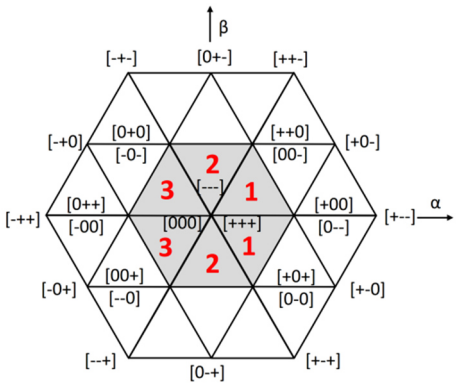
Until now, only the case of a thermal overload of the upper leg of phase U has been considered exemplarily. In case that the temperature in a different leg of the inverter exceeds the threshold value defined for the operation of ALE, the scheme described above has to be extended accordingly.

In the case of low modulation index the considerations of the sections 3.1.1, 3.1.2 and 3.1.3 have to be applied to the other upper or lower legs of the inverter. Figure 26 shows the cases for the elimination of one, two or three switching states from the switching matrix for relieving the upper and lower legs of the phases U, V and W.

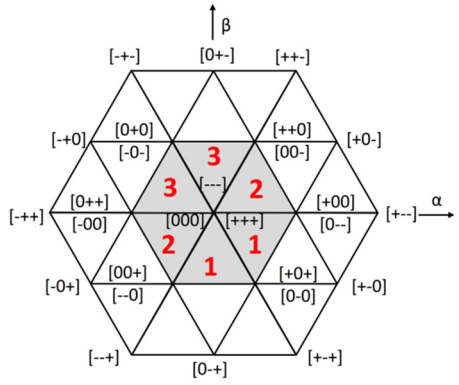
In case of the range of high modulation index, the generalization can be easily attained by defining operational maps for the different legs as depicted in Figure 27. As in the previous analysis, the thermal overload occurs in the upper leg of phase U and the reference-voltage space vector enters the blue sectors of Figure 27 (a), the ALE procedure is applied. If the malfunction occurs in the lower leg of the same phase, the operation map of Figure 27 (b) is accordingly applied and the ALE procedure is started, when the voltage space vector enters the blue region. In the same way the control considers the thermal situation in the upper and lower legs of the other two phases V and W as shown in Figure 27 (c) to Figure 27 (f).



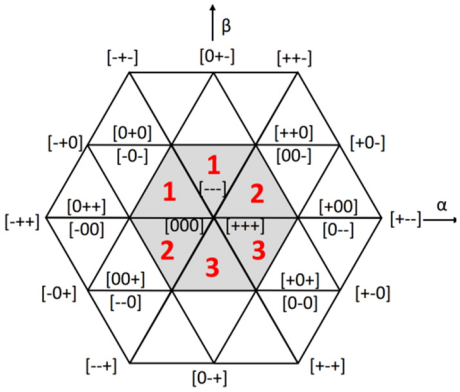
(a) Upper leg of phase U



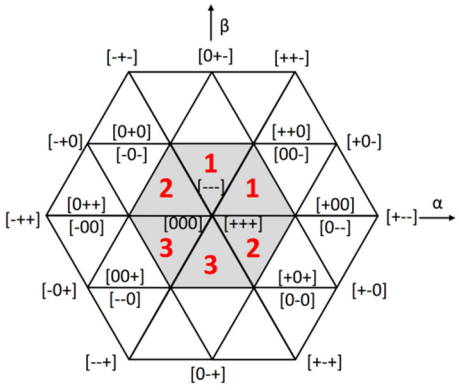
(b) Lower leg of phase U



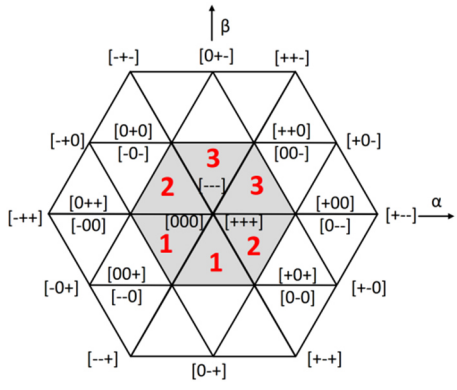
(c) Upper leg of phase V



(d) Lower leg of phase V

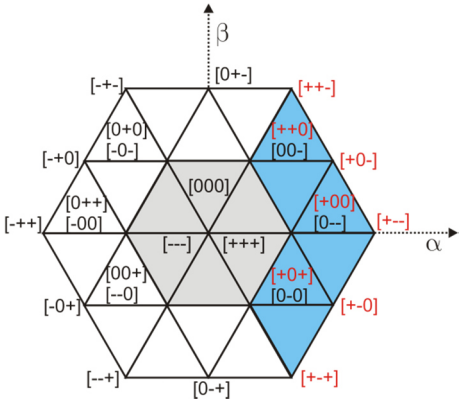


(e) Upper leg of phase W

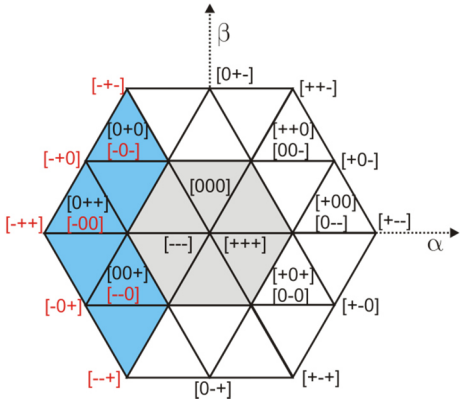


(f) Lower leg of phase W

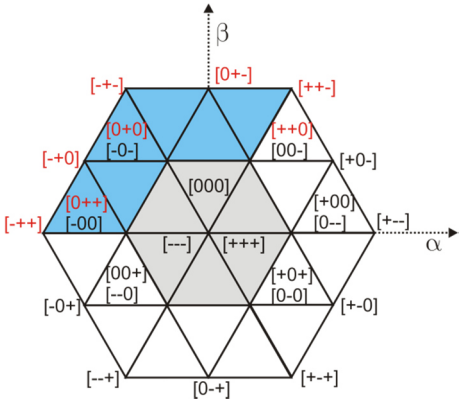
Figure 26: Operational map for the modified PWM with ALE in the range of low modulation index for reducing the losses in one inverter leg. The red digits indicate the number of switching states to be removed from the switching sequence.



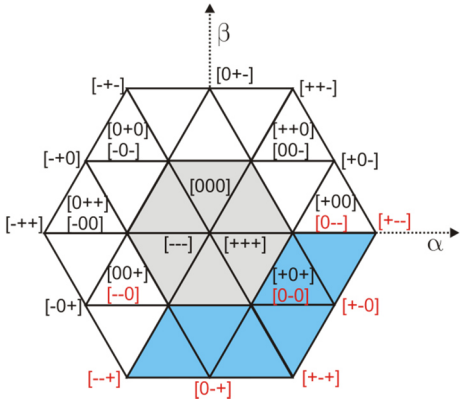
(a) Upper leg of phase U



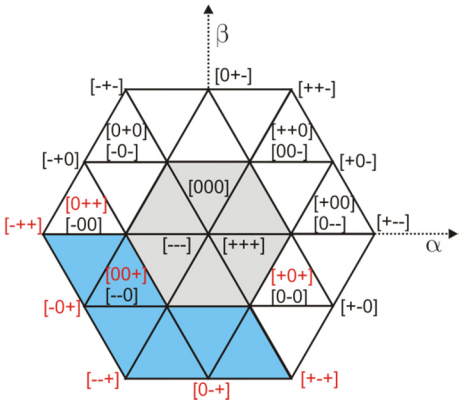
(b) Lower leg of phase U



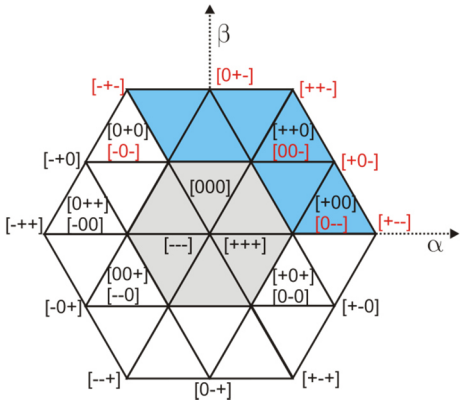
(c) Upper leg of phase V



(d) Lower leg of phase V



(e) Upper leg of phase W



(f) Lower leg of phase W

Figure 27: Operational map for ALE in high modulation index range for reducing the losses in the affected leg

3.4 Limits of proposed modified PWM

It is evident that with the proposed PWM Active Lifetime Extension for all the semiconductors of the inverter cannot always be achieved.

In case that the lower switch in an upper leg (e.g. S2) or the upper one in a lower leg (e.g. S3) of one phase exhibits a thermal overload, PWM with ALE will become active. As the simulations and measurements show, it is only capable of obtaining a significant reduction of the losses in one of the inner switches if the inverter is operated in the range of low modulation index.

If the thermal overload takes place in the outer switches, e.g. S1 or S4, the PWM with ALE can be applied and achieves a substantial reduction of the losses in both ranges of the modulation index.

The benefit of the proposed PWM with ALE is unfortunately limited due to the physics of the inverter, yet it reaches the maximum of technically feasible protection or Active Lifetime Extension.

3.5 Summary of chapter

This chapter describes the proposed changes that have to be carried out in the PWM algorithm in order to redistribute the losses from an overheated switch to the others that still have an acceptable junction temperature due to a well-functioning cooling. The necessary modifications of the PWM are based on the principle that those switching states that produce losses in the affected switches have to be removed from the switching sequences and replaced by the redundant ones so that the stressed switch is thermally relieved. Since the number of switching states that can be removed from a particular switching sequence is associated with the location of the reference voltage vector on the complex α,β-plane, the different sectors of operation have to be examined. Several solutions for the range of low and for the range of high modulation index are developed and maps for the operation of the modified PWM with ALE are proposed. For the range of high modulation index the impact of the modified PWM on

both switching and conduction losses in the affected switch has to be included into the analysis.

4 Experimental results

4.1 Experimental set-up

4.1.1 Control electronics

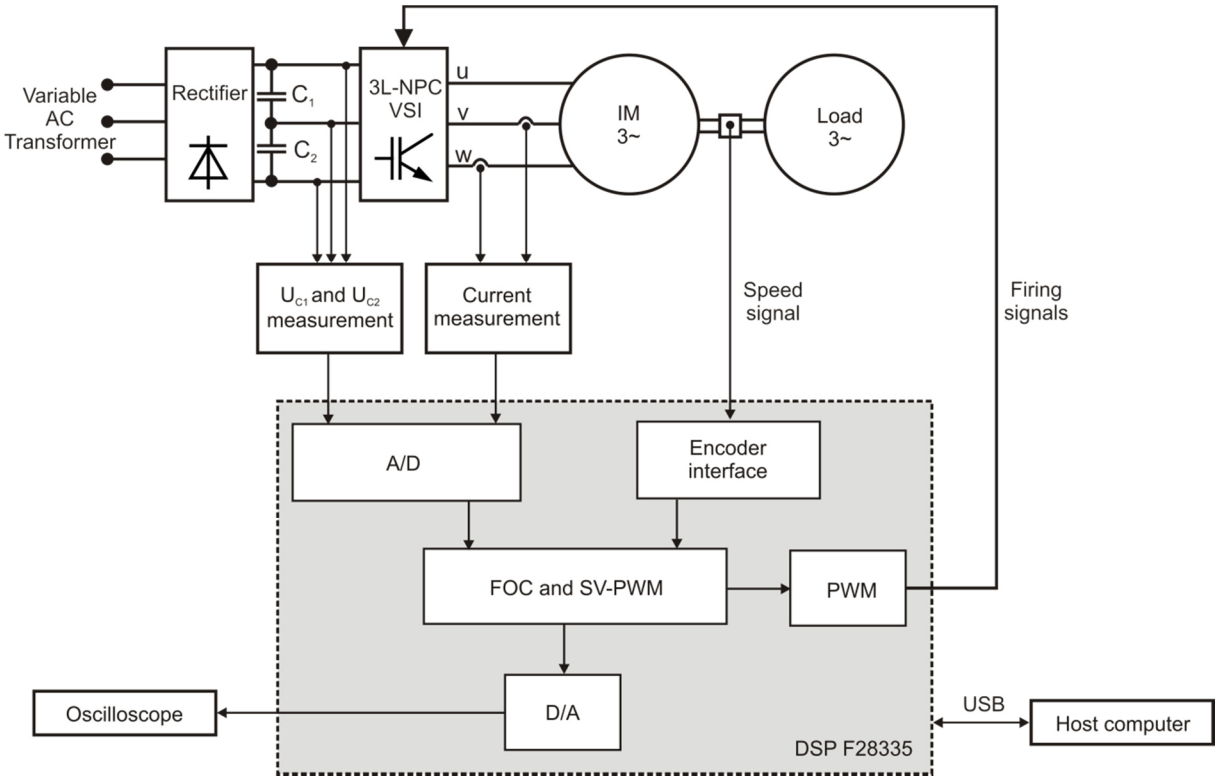


Figure 28: Laboratory set-up

The proposed modulation strategy was implemented on a DSP eZdsp^{TM} F28335 card. A block diagram of the experimental set-up is shown in Figure 28. For the monitoring of the different variables and signals, four Digital-to-Analog (D/A) channels with 11-Bit resolution were installed. The gate signals for the inverter switches were transmitted from the PWM outputs of the DSP to the drivers by means of optical fibers in order to be less susceptible to EMI. The sensors are interfaced with the DSP via 8 Analog-to-Digital (A/D) channels with 12-Bit resolution.

4.1.2 Inverter

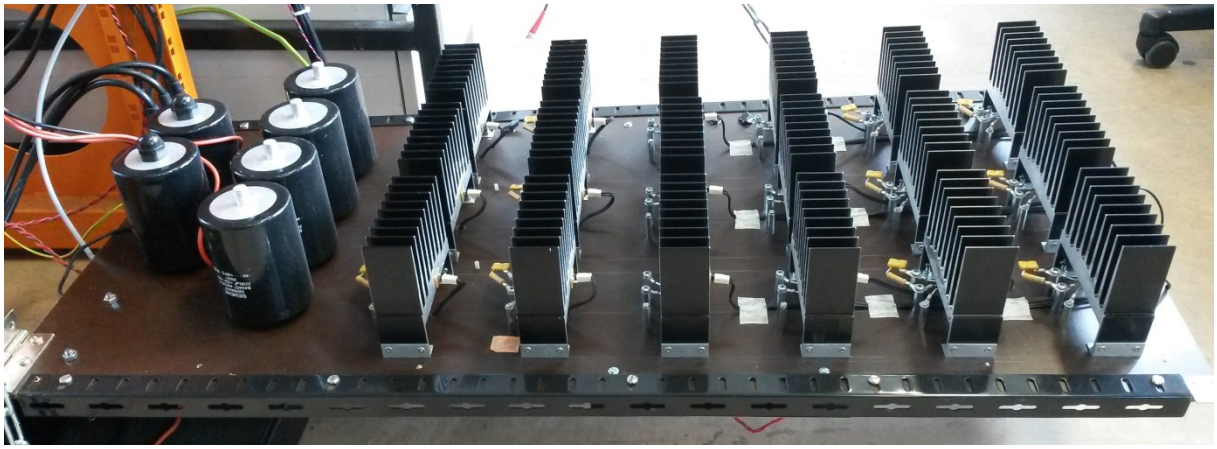


Figure 29: Arrangement of the heatsinks in the 3L-NPC VSI

The 3L-NPC VSI (560 V, 37 A rms, 5 kHz) was especially designed with 18 separated heatsinks and with a lay-out as shown in Figure 29. Each phase of the inverter consists of 4 IGBTs with their antiparallel diodes (IXGR72N60A3H1, 600 V, 52 A) and 2 neutral-point diodes (DSEP 60-12AR, 1200 V, 60 A). Each heatsink (R_{ha} = 1.1 $K \cdot W^{-1}$) is dedicated to one switch and is equipped with a temperature sensor (Pt1000), thus the thermal losses of each semiconductor device can be easily estimated by sensing the temperature of the heatsink in the steady-state.

The IGBTs utilized in the downsized laboratory set-up have characteristics for optimized conduction losses [52], therefore they can replicate in a suitable way the thermal behavior of the high-power IGBTs.

The 3L-NPC VSC feeds a 15 kW induction motor (400 V, 31.1 A, 1455 min^{-1}) and as a brake a 21-kW field-oriented controlled motor drive was used. The parameters of the lab drive system are given in 9.1. Figure 30 shows the set of machines with a torque gauge in the middle.

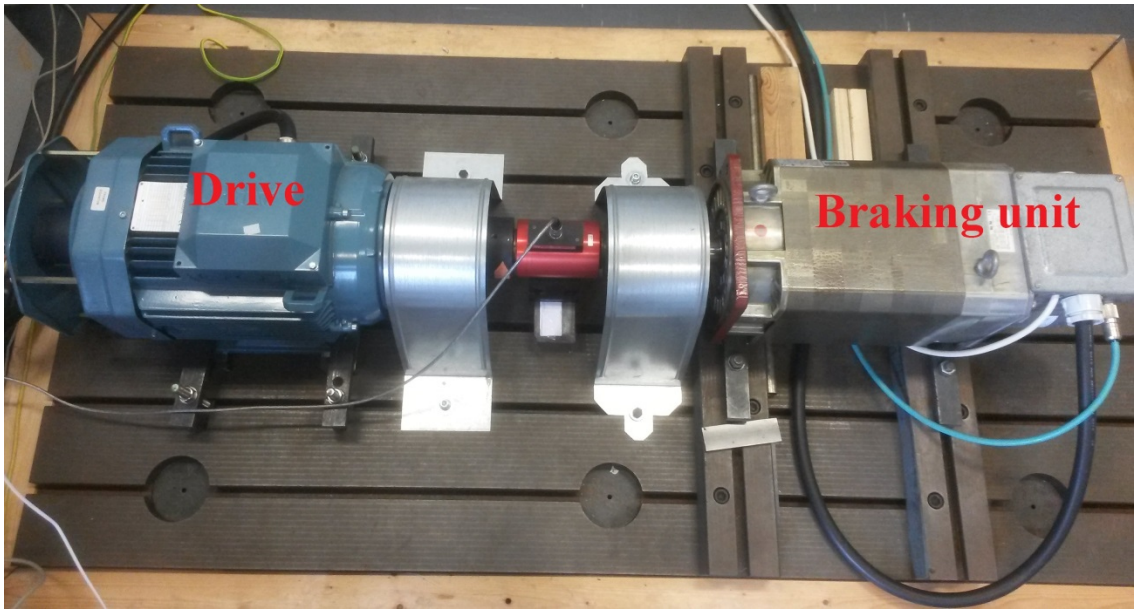


Figure 30: Machine set in the laboratory set-up

4.1.3 Estimation of losses in each semiconductor device

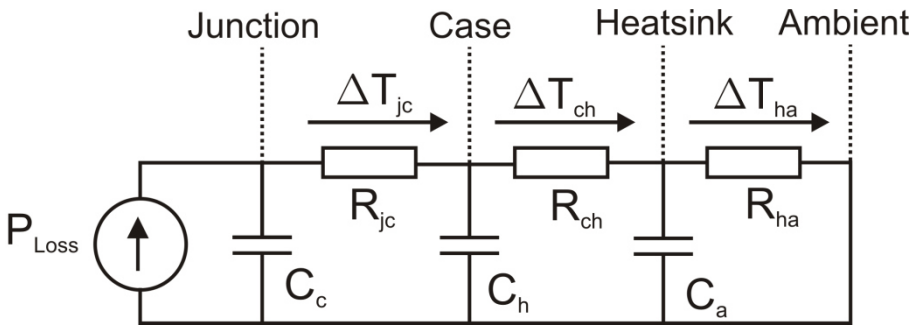


Figure 31: Thermal model of the semiconductor switch.

Figure 31 depicts the introduced thermal model (Cauer equivalent network) of a semiconductor device mounted on separated heatsink [63]. The term R refers to a thermal resistance and the term C to a thermal capacitance of a material layer (silicon, PCB from AL-N or plastic casing, etc.). The parameters of the model can be calculated based on the datasheet (curve-fitting from the transient thermal resistance curve). The junction temperature T_J of the switch is given by:

$$T_j = \Delta T_{jc} + \Delta T_{ch} + \Delta T_{ha} + T_{Ambient}\,, \tag{44}$$

ΔT refers to the temperature difference between two adjacent environments, where the subscripts *jc*, *ch* and *ha* stand for *junction-to-case*, *case-to-heatsink* and *heatsink-to-ambient,* respectively. Applying the nodal rule, the total losses of the semiconductor device P_{Loss} can be calculated as:

$$P_{Loss} = C_{jc}\frac{d}{dt}\Delta T_{jc} + C_{ch}\frac{d}{dt}\Delta T_{ch} + C_{ha}\frac{d}{dt}\Delta T_{ha} + \frac{\Delta T_{ha}}{R_{ha}}. \tag{45}$$

In steady state, the time-derivative quantities are assumed to be zero and the total losses P_{Loss} can be estimated due to:

$$P_{Loss} \approx \frac{\Delta T_{ha}}{R_{ha}}. \tag{46}$$

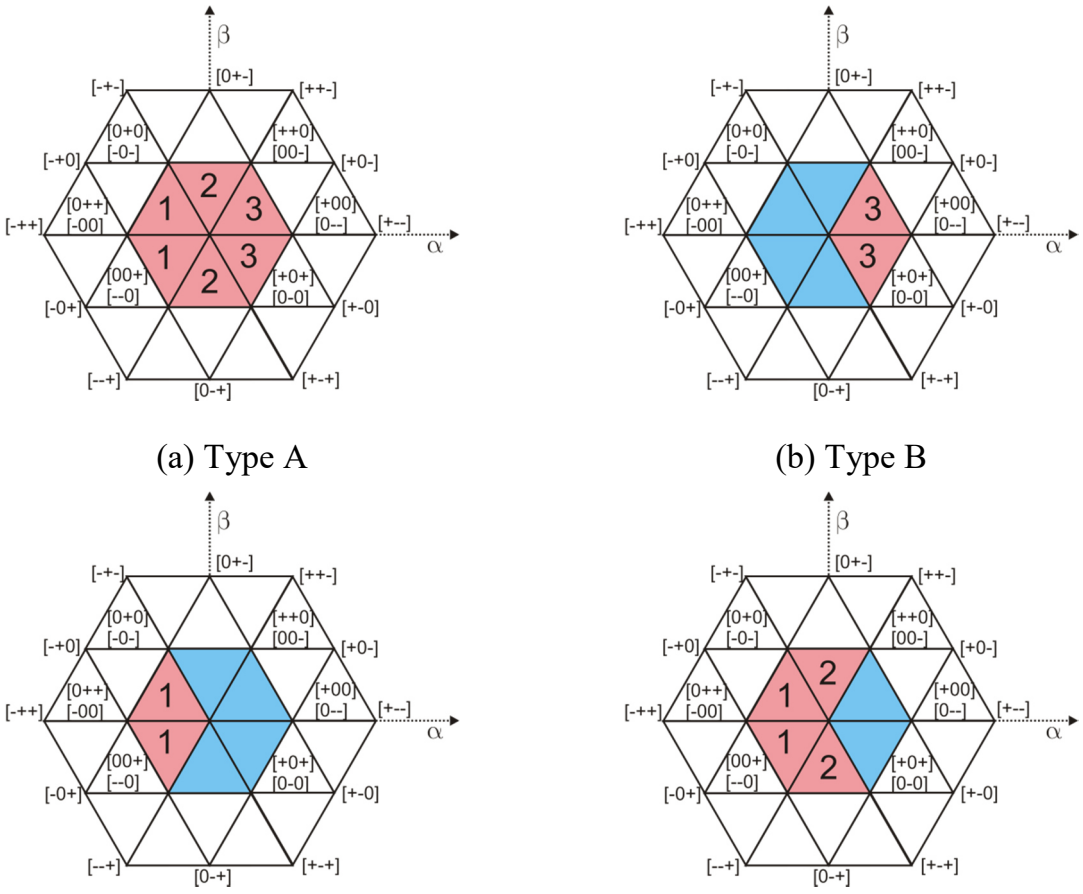
The temperature difference ΔT_{ha} can be easily obtained by measuring the temperatures of the heatsink and the ambient air; R_{ha} is the thermal resistance of the heatsink as obtained from the data-sheet. In order to reduce the thermal coupling among the switches due to the air convection, the heatsinks are laid down in the horizontal position as shown in Figure 29. The measurement of the heat-sink temperature is performed after reaching the thermal steady state, in which no further increase of temperature can be registered.

The temperature measurement is carried out with Pt1000 Resistance Temperature Detectors that feature higher accuracy, linearity, stability over long time and temperature range, providing better immunity against EMI than thermistors, thermocouples or diodes.

4.2 Results of measurements

4.2.1 Performance of PWM with ALE in the range of low modulation index

For the analysis of the performance of the PWM with ALE in the range of low modulation index different measurements were carried out. First the 3L-NPC VSI was operated with modulation index $m = 0.46$, fundamental frequency $f_S = 21$ Hz and the induction machine was loaded with a torque $M_{load} = 0.4 \cdot M_{rated}$.



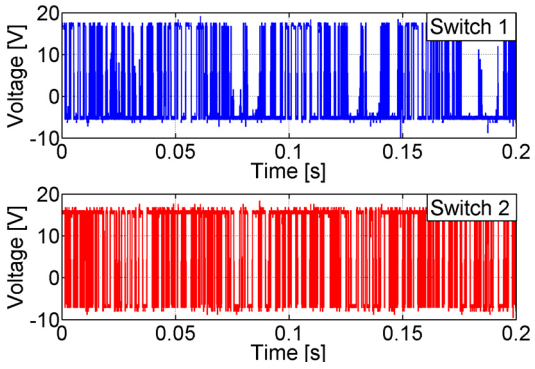
(a) Type A (b) Type B

(c) Type C (d) Type D

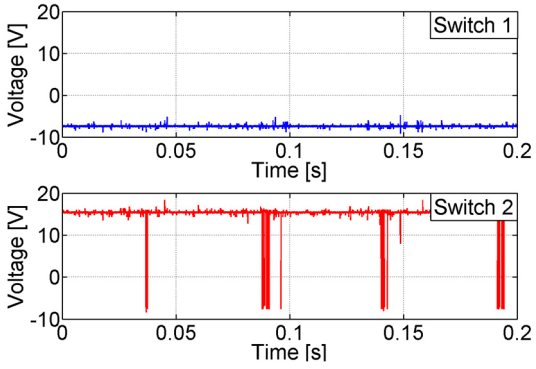
Figure 32: Operational maps for the range of low modulation index. For the areas in blue conventional D-PWM is applied, for those in red PWM with ALE. The digits indicate the number of switching states to be removed from the calculation to relieve the upper leg of phase U.

As mentioned in 3.1, PWM with ALE can be applied to the whole range of low modulation index, because the employed three nearest vectors are redundant. The corresponding operational map is shown in Figure 32 (a), which is designed for the application of PWM with ALE to reduce the losses in switch 1 and in switch 2. The use of such an operational map yields a significant reduction of losses in the affected switching devices, however it causes very large distortion of the neutral-point voltage. In order to minimize the distortion of the neutral-point voltage, the use of the PWM with ALE should be limited to a predefined area. In the following, three different operational maps of Type B, Type C and Type D are proposed for the range of low modulation index and are shown in Figure 32 (b) thru Figure 32 (d), respectively. The digit in black refers to the number of switching states, which have to be removed from the calculation in order to relieve switch 1 and switch 2 (conf. 3.1). The more switching states are excluded from the calculation, the larger is the distortion of the neutral-point voltage. The regions in blue indicate the regions, in which the normal D-PWM is used.

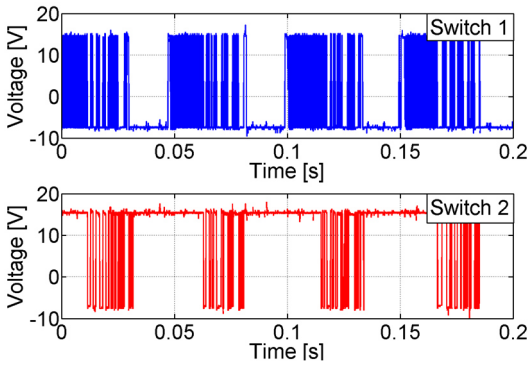
The gate signals U_{GE} of switch 1 and of switch 2 – using different operational maps – were measured by employing differential voltage probes and are shown in Figure 33 (a) thru Figure 33 (e), respectively. The IGBTs are turned on with $U_{GE} = 15$ V and turned off with a negative voltage $U_{GE} = -7$ V. The negative voltage U_{GE} is necessary to mitigate the parasitic turn-on effect of IGBT due to the Miller-capacitor effect [56]. Figure 33 (a) shows the pulses of switch 1 (blue trace) and switch 2 (red trace) in normal operation mode with D-PWM.



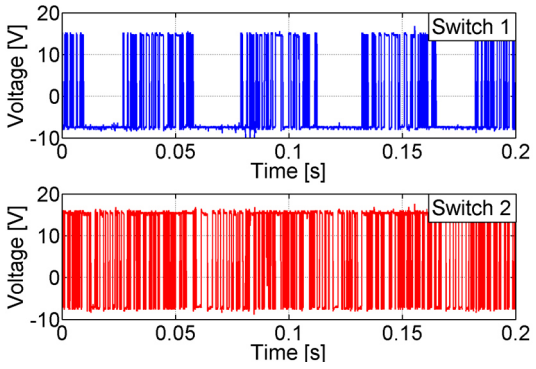
(a) Operation with normal D-PWM



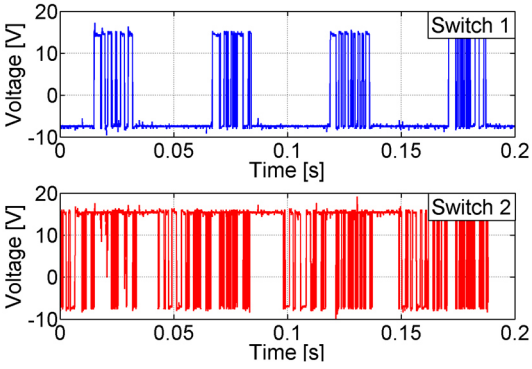
(b) Operational map of type A



(c) Operational map of type B



(d) Operational map of type C



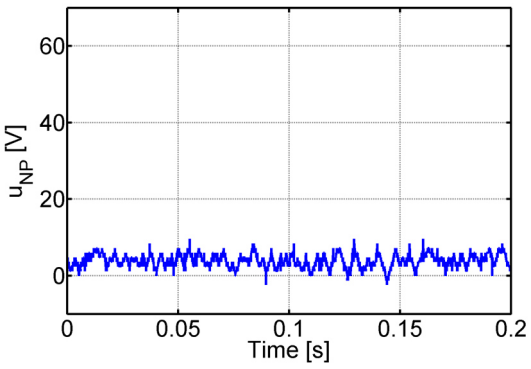
(e) Operational map of type D

Figure 33: Gate signals U_{GE} for switch 1 (blue) and for switch 2 (red), modulation index $m = 0.46$, fundamental frequency $f_S = 21$ Hz and for different operation modes

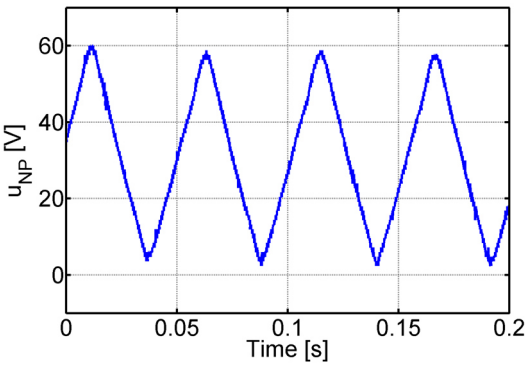
If the operational map in Figure 32 (a) is used, switch 1 remains turned off, its gate signal is depicted as the blue trace in Figure 33 (b). In this case, all the switching states connecting phase U to the *positive* DC rail are excluded from the modulation. Yet the phase U can still be connected either to the neutral point or to the negative DC rail. The exclusion of switching states connecting phase U to the positive DC rail reduces the number of possible switching states with positive common-mode voltage. In order to keep the imbalance of the neutral-point voltage as small as possible, the switching states connecting phase U to the neutral point are preferred. As consequence, switch 2 is mostly turned on and clamped to the neutral point. The red trace in Figure 33 (b) depicts the gate signal of the switch 2.

Figure 33 (c) thru Figure 33 (e) show the gate signals of switch 1 and of switch 2 when employing the other operational maps Type B thru Type D, respectively. By analyzing the gate signal of switch 1, it can be seen that this device is turned off periodically for 120°, when the operational map depicted in Figure 32 (b) is used. For an operation according to the operational maps depicted in Figure 32 (c) and Figure 32 (d), switch 1 stays off for 120° and 240° electrical degree, respectively. In case of switch 2, the clamping duration varies due to the load, since this switch is needed not only for the connection of phase U to the positive DC rail, but also to the neutral point. Therefore, the removal of the switching states connecting phase U to the positive DC rail reduces the conduction losses of the switch 2, but it does not exclude the device completely from the modulation.

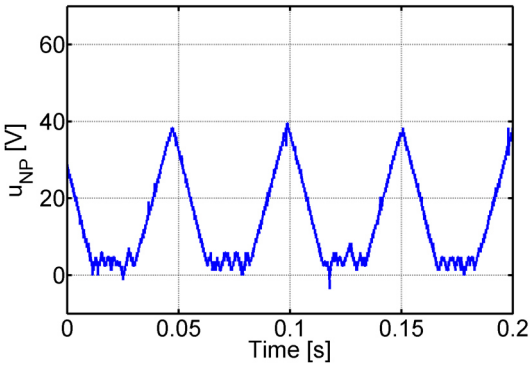
Figure 34 (a) presents the waveform of the neutral-point voltage for the normal operation with D-PWM. As expected for the low modulation index range, the neutral-point voltage ripple is small thanks to the absence of the medium voltage space vector (cfg. 2.5.1) and to the use of only redundant voltage space vectors. The small offset in the neutral-point voltage is caused by the non-ideal behavior of the components used in the laboratory set-up and probably inaccuracies of the execution of the pulse pattern [41].



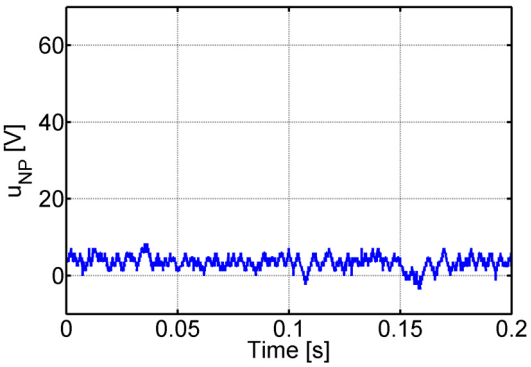
(a) Normal D-PWM



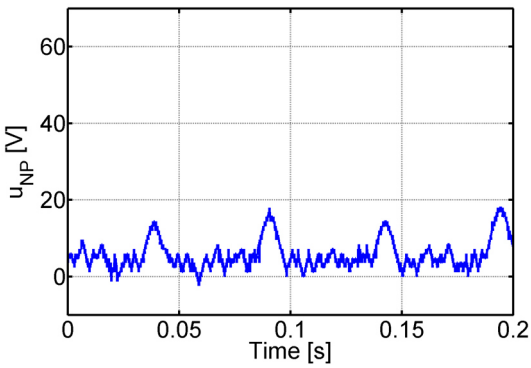
(b) Operational map of PWM with ALE for type A



(c) Operational map of PWM with ALE for type B



(d) Operational map of PWM with ALE for type C



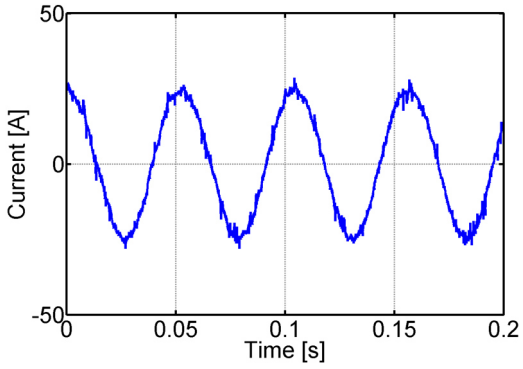
(e) Operational map of PWM with ALE for type D

Figure 34: Measured neutral-point voltage, modulation index m = 0.46, 40% rated torque, fundamental frequency $f_S = 21$ Hz with $U_{DC} = 560$ V

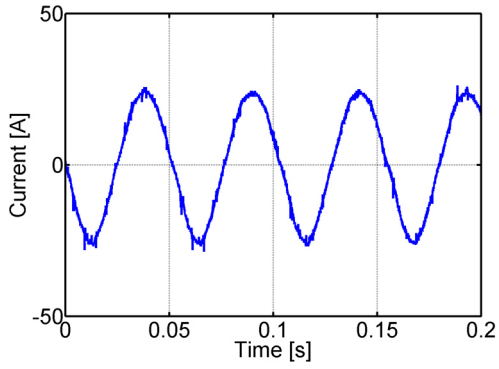
If the operational map of type A shown in Figure 32 (a) is used, the control of the neutral-point voltage is strongly affected and the voltage ripple becomes very large as seen in Figure 34 (b).

Figure 34 (c) thru Figure 34 (e) show the changes of the ripple in the neutral-point voltage are if the inverter is operated in the modes corresponding to Figure 32 (b) thru Figure 32 (d), respectively. The use of operational map of type B reduces the control quality of the neutral-point voltage, since a group of three switching states has to be excluded from the calculation. As a result of the fewer switching states removed from the calculation the ripple of the neutral-point voltage by applying operational map C is much smaller, although switch 1 in both cases i.e. using operational maps type B or type C is clamped for 120°. Hence, it is important to point out that the magnitude of the ripple of the neutral-point voltage does not only depend on the clamping duration of the D-PWM, but also on the utilized switching pattern. This statement can be confirmed by analyzing the case of applying operational map D, in which switch 1 is turned off for 240° electrical degree. Here, the neutral-point voltage ripple is still smaller as compared with the case of operational map B, in which the clamping duration of switch 1 is only 120°.

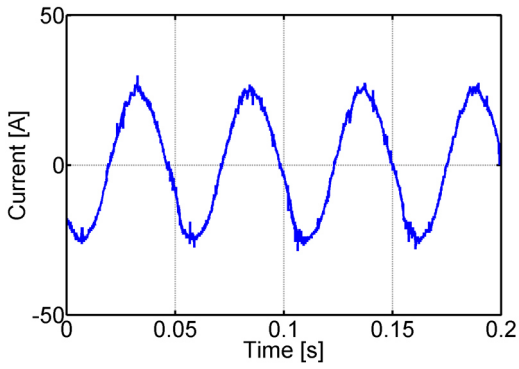
Figure 35 (c) thru Figure 35 (e) show the measured load currents by employing the other operational maps Type B thru Type D, respectively.



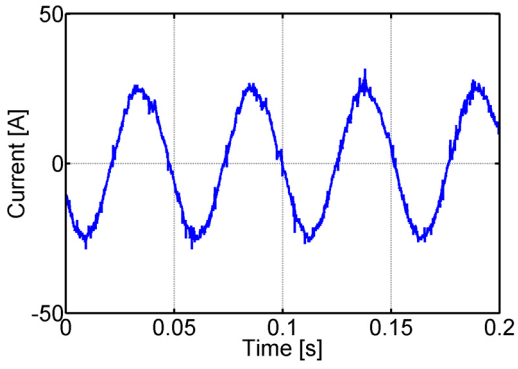
(a) Normal D-PWM



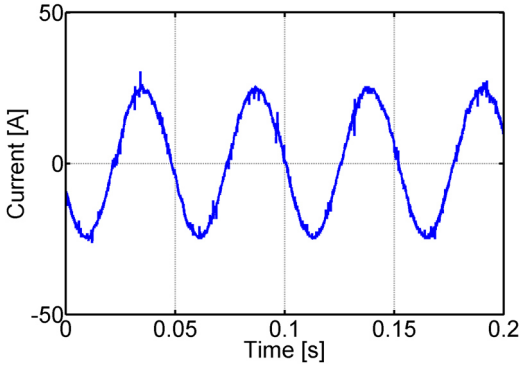
(b) PWM with ALE for type A



(c) PWM with ALE for type B



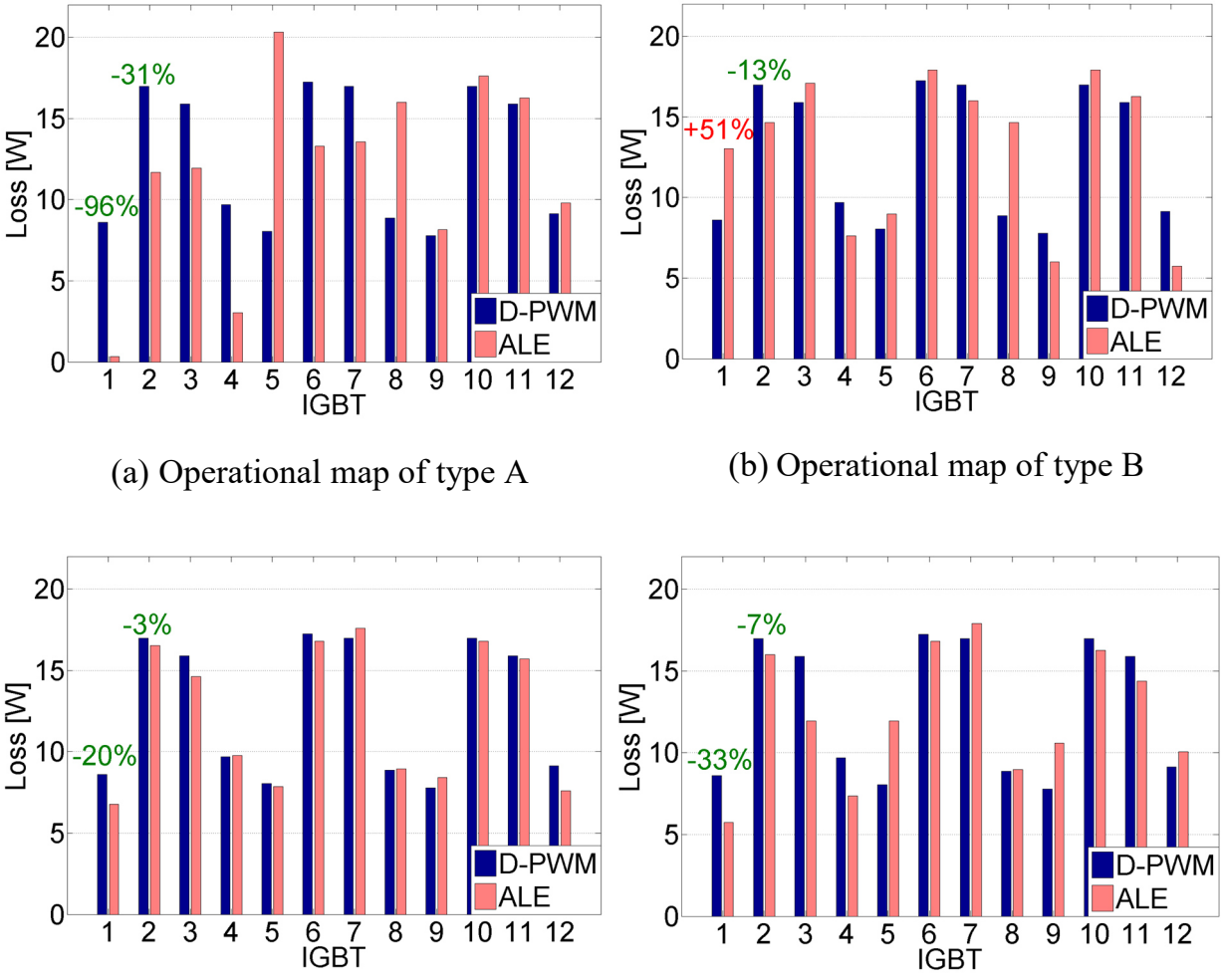
(d) PWM with ALE for type C



(e) PWM with ALE for type D

Figure 35: Measured load current, modulation index m = 0.46, 40% rated torque, fundamental frequency $f_S = 21$ Hz with $U_{DC} = 560$ V

Figure 36 shows the distribution of the overall losses in the IGBTs 1..12 (see Figure 1) under the different operational conditions: D-PWM (columns in blue) and PWM with ALE (columns in red). Figure 36 (a) shows a significant reduction of losses in switch 1. Switch 2 is also relieved thanks to the application of the modified PWM with ALE and exhibits a reduction of losses by 31%.



(a) Operational map of type A

(b) Operational map of type B

(c) Operational map of type C

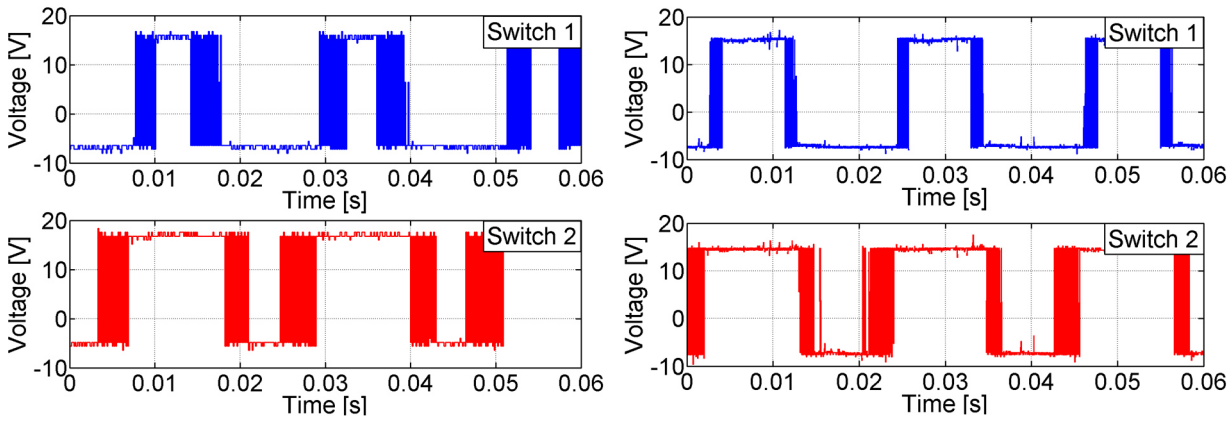
(d) Operational map of type D

Figure 36: Total loss distribution in the switches of the inverter for modulation index $m = 0.46$, 40% rated torque, D-PWM (columns in blue) and ALE (columns in red)

4.2.2 Performance of PWM with ALE in the range of high modulation index

As explained in the previous sections, the realization and implementation of the modified PWM with ALE depends on the range of modulation in which the inverter is operated. In the following, the performance of the PWM with ALE is examined for an operation of the 3L-NPC VSI with $m = 0.95$, feeding an induction machine loaded with its rated torque. The region of operation corresponds to the one depicted in blue in Figure 24, which is intended for the application of the PWM with ALE in the range of high modulation index and is the switching patterns are optimized aiming at reduction of losses of the switch 1.

Figure 37 (a) shows the measured gate signals of switch 1 and switch 2 for the case of normal operation. The zone free of pulses in the middle of the pulse patterns corresponds to the clamping duration, in which the device remains switched off. Figure 37 (b) shows the gate signals, when the PWM is modified by ALE. It is obvious that the effective switching frequency of switch 1 decreases significantly, since the clamping duration becomes larger as compared with the case shown in Figure 37 (a).

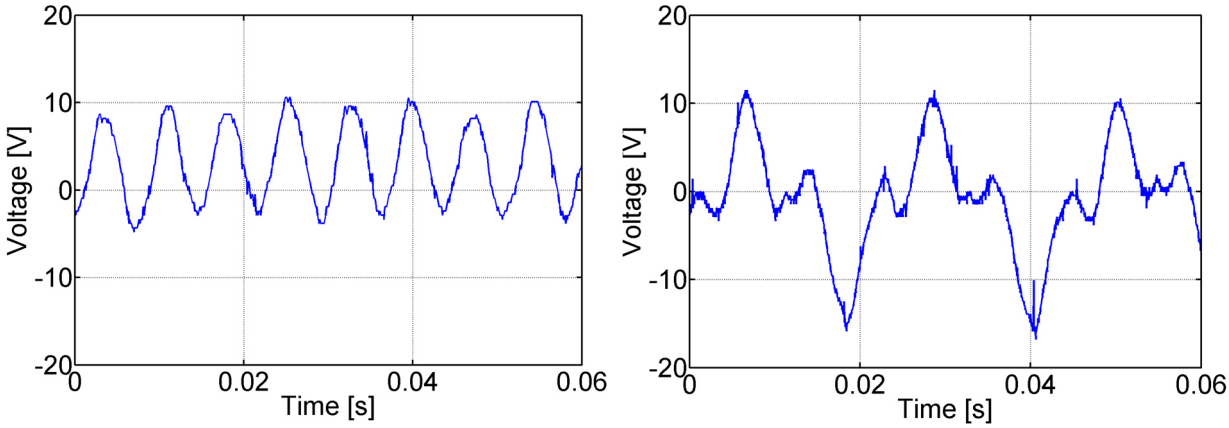


(a) Normal D-PWM (b) PWM with ALE

Figure 37: Gate signals U_{GE} of switch 1 (blue) and switch 2 (red) for $m = 0.95$, fundamental frequency $f_S = 45.9$ Hz and rated torque

Figure 38 (a) shows the measured neutral-point voltage under normal operation, which shows a low-frequency ripple and is typical for the operation of the inverter in the

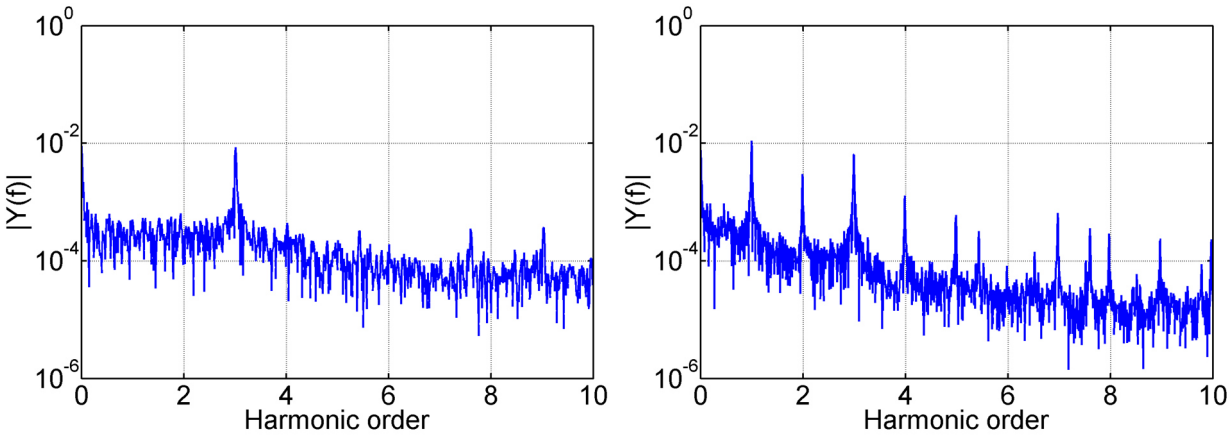
range of high modulation index. It is well known that the low-frequency ripple of the neutral-point voltage is mostly caused by the use of the medium voltage space vectors, which is unavoidable in this range. In case of an operation with a modified PWM with ALE, the ripple of neutral-point voltage becomes larger and is depicted in Figure 38 (b).



(a) Normal D-PWM (b) PWM with ALE

Figure 38: Results of measurement of the neutral-point voltage for m= 0.95, fundamental frequency $f_S = 45.9$ Hz and rated torque of the induction machine at $U_{DC} = 560$ V

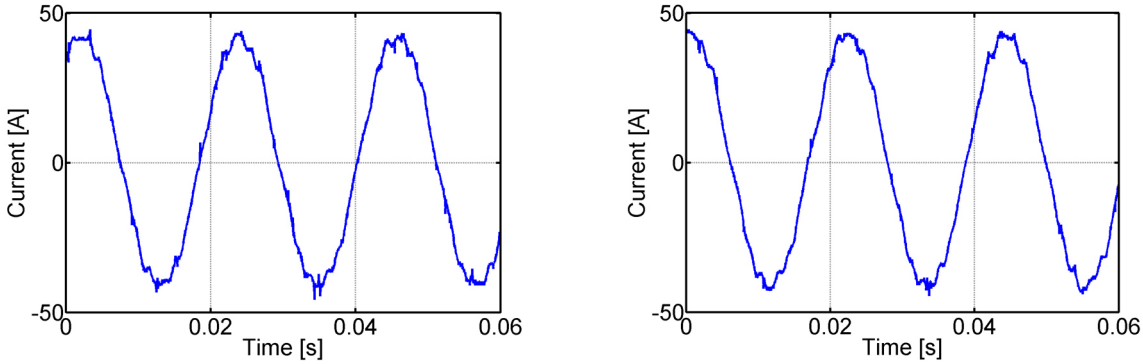
The spectrum of the normalized measured neutral-point voltage u_{NP} under normal operation shows a dominant 3rd harmonic component in Figure 39 (a). The spectrum of the measured neutral-point voltage in case of ALE operation is depicted in Figure 39 (b). The spectrum contains also a 3rd harmonic component, but also additional spectral components of 1st, 2nd, 4th, 5th and 7th order. The DC part and the odd components of 1st, 5th, 7th etc. are called forth by the modified PWM with ALE, which affects the control of the neutral-point voltage. The even harmonics, i.e. the 2nd and the 4th, appear due to the presence of an offset voltage in the neutral-point voltage [49].



(a) Normal D-PWM (b) PWM with ALE

Figure 39: Spectrum of the measured neutral-point voltage U_{NP} for $m = 0.95$, fundamental frequency $f_S = 45.9Hz$ and rated torque of the induction machine

Figure 40 presents the measured load current under normal operation and in case of operation with PWM with ALE.



(a) Normal D-PWM (b) PWM with ALE

Figure 40: Measured load current for $m = 0.95$, fundamental frequency $f_S = 45.9$ Hz and rated torque of the induction machine

The total loss distribution in the switching devices of the 3L-NPC VSI is shown in Figure 41. The losses of switch 1 have been reduced significantly by 37% at expense of higher losses in the devices 5, 8 and 9. Nevertheless it can be seen that the modified PWM with ALE strategy does not reduce the losses of switch 2 considerably. This is a clear limitation of the proposed strategy in the range of high modulation index.

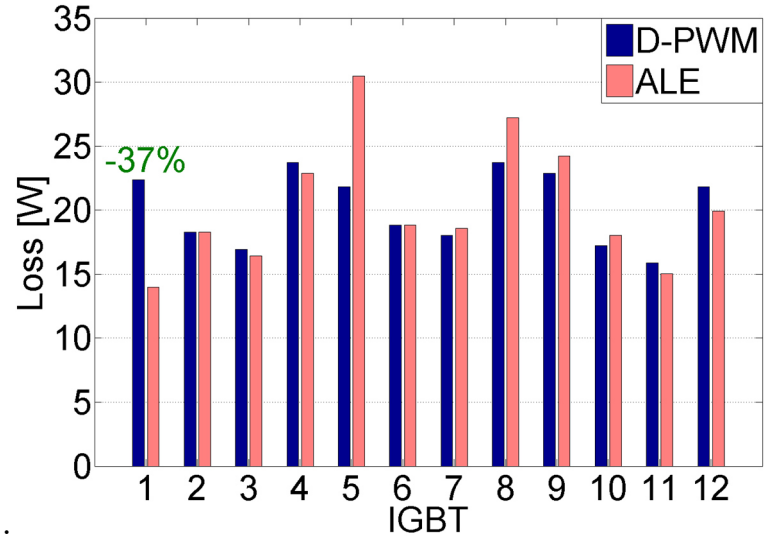


Figure 41: Total loss distribution in the switches of the 3L-NPC VSI for $m = 0.95$ and rated torque of the induction machine. The columns in blue stand for the case of normal D-PWM, columns in red for PWM with ALE.

Figure 42 shows the amount of loss reduction in switch 1, where $P_{Loss,Normal}$ refers to the total losses of switch 1 under normal operation with D-PWM and $P_{Loss,ALE}$ denotes the total losses of switch 1 in case of operation with the modified PWM with ALE. A remarkable reduction of the overall losses of at least 37% can be stated. The performance of PWM with ALE varies strongly due to many factors: the characteristic of used semiconductor devices, the selection of the gate resistance, the switching frequency, the operation point (modulation index and power factor), the stray inductance, etc. Therefore, here only the fundamental relationships can be illustrated for relevant operational conditions.

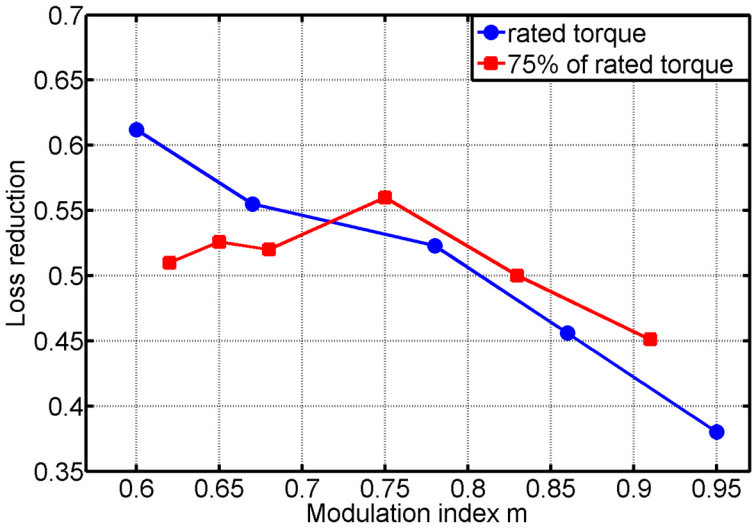
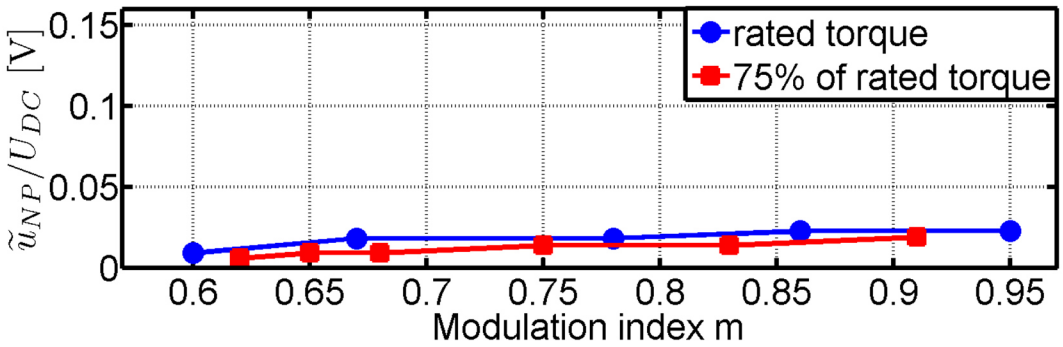
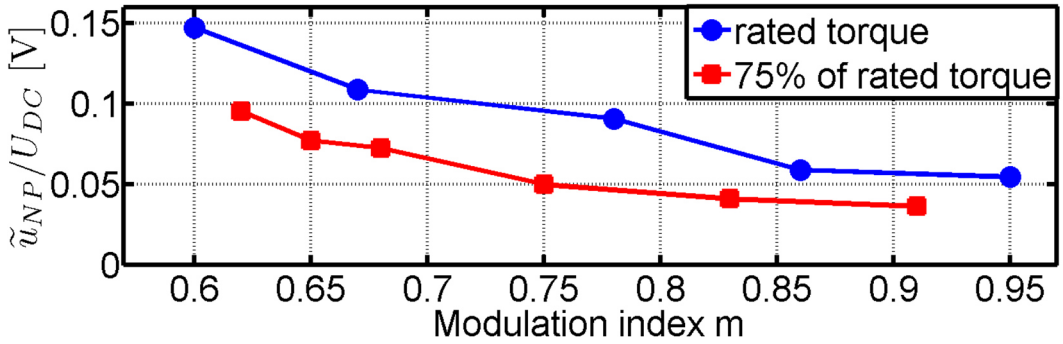


Figure 42: Loss reduction $\frac{P_{Loss,Normal}-P_{Loss,ALE}}{P_{Loss,Normal}}$ of switch 1 by applying PWM with ALE

Figure 43 (a) and Figure 43 (b) show the ripple of the normalized neutral-point voltage $\tilde{u}_{NP}/U_{DC}$ for the operation of the inverter with D-PWM and with the modified PWM with ALE. The neutral-point voltage ripple shows a clear tendency in case of the modified PWM: the higher the modulation index, the smaller the amplitude of the ripple. In normal operation the ripple behaves the other way, as is depicted in Figure 43 (a). Regarding the impact of the modified PWM with ALE on the DC-link capacitors, in the experimental set-up a temperature rise of maximum 10 K could be measured during the operation with the modified PWM.



(a) Ripple (peak-to-peak) of neutral-point voltage with normal DPWM



(b) Ripple (peak-to-peak) of neutral-point voltage when using PWM with ALE

Figure 43: Performance of modified PWM for different operational points. The curve in blue stands for operation of the induction machine at rated torque, in red for 75% rated torque

4.2.3 Reduction of losses in one inverter phase in the range of high modulation index by using modified PWM

Until now, the proposed PWM enhancement was examined for the reduction of losses in one (upper or lower) leg of one phase; however the procedure can also be applied to relieve both legs of the same phase. The corresponding operational map is shown in Figure 44.

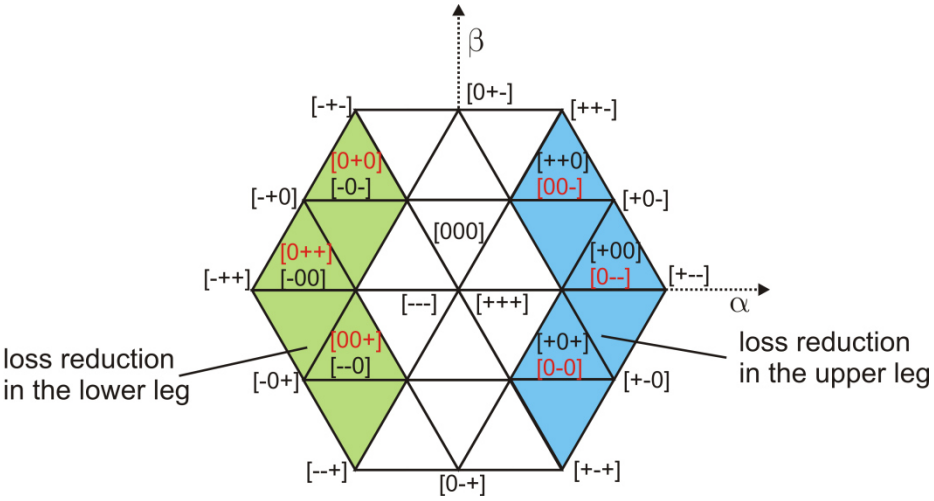
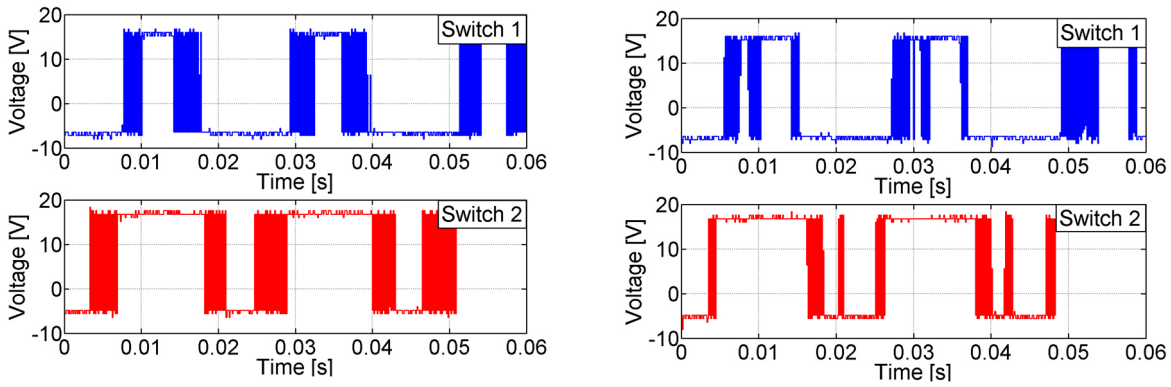


Figure 44: Operational map for the reduction of losses in phase U. The blue region corresponds to the loss reduction in the upper leg, green for the lower leg.

The gate signals of the switches 1 and 2 are shown in Figure 45, where the 3L-NPC VSI is operated at a modulation index $m = 0.95$ and the induction machine fed by the inverter is loaded with *rated torque*. Due to the symmetry, the gate signals of switches 3 and 4 do not need to be shown. Compared with the case of D-PWM, the width and the placement of the zone free of pulses change if applying modified PWM with ALE.

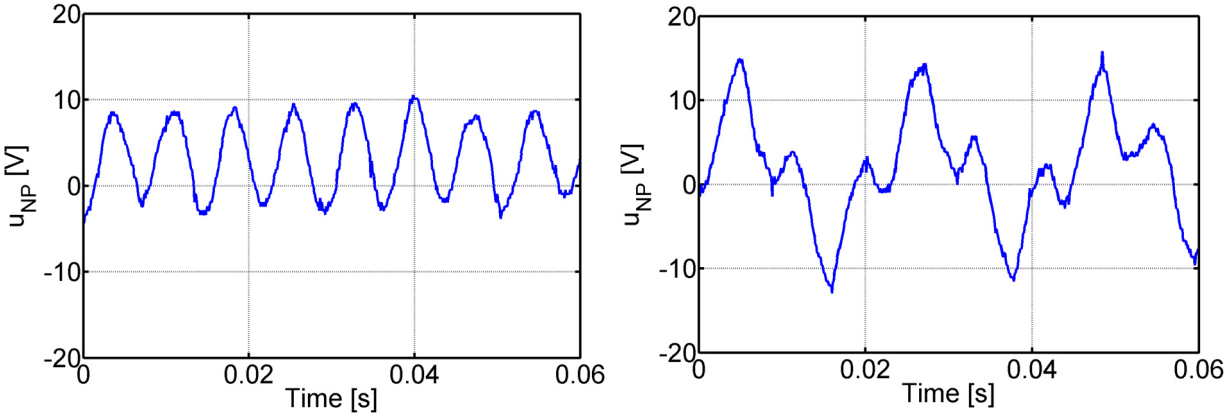


Normal D-PWM

PWM with ALE for loss reduction on IGBTs 1, 2, 3 and 4

Figure 45: Gate signals pulses of switches 1 and 2 for $m = 0.95$, fundamental frequency $f_S = 45.9$ Hz and rated torque

Figure 46 depicts the measurement of the voltage of the neutral-point voltage for both cases: normal operation and operation with modified PWM with ALE.

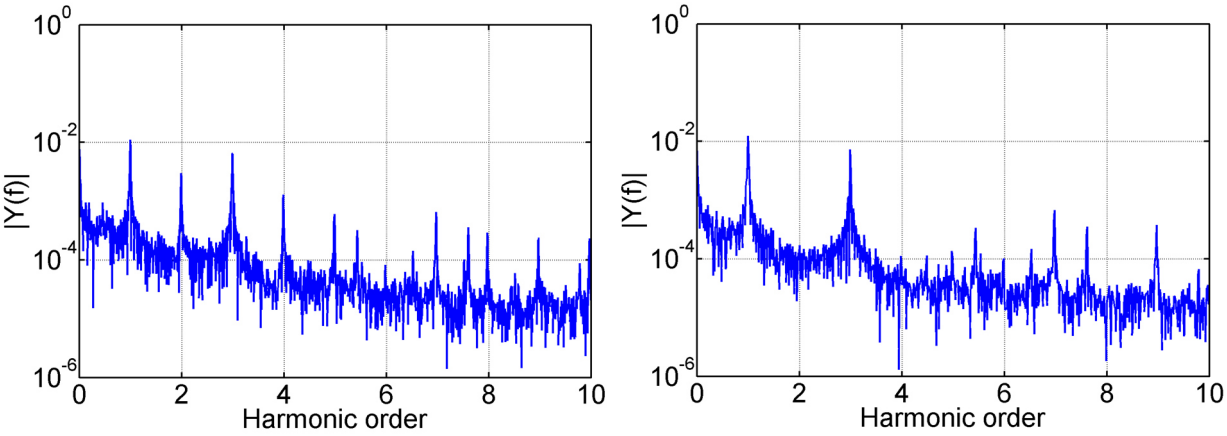


(a) Normal D-PWM

(b) PWM with ALE to reduce the losses of phase U

Figure 46: Voltage of the neutral point for m= 0.95, fundamental frequency $f_S = 45.9$ Hz and rated torque of the fed induction machine

Figure 47 (a) shows the spectrum of the normalized neutral-point voltage in case that modified PWM is used for the reduction of losses in the upper leg of phase U and Figure 47 (b) for the case that a reduction of the losses in both legs of phase U is aimed at.



(a) Modified PWM aiming at reduction of losses of switches 1 and 2

(b) PWM with ALE aiming at reduction of losses of switches 1, 2, 3 and 4

Figure 47: Spectrum of the normalized neutral-point voltage for m= 0.95, fundamental frequency $f_S = 45.9Hz$ and rated torque of the fed induction machine

The losses in the switches of the 3L-NPC VSI are compared in Figure 48. Both the devices switch 1 and switch 4 are relieved thanks to the application of modified PWM with ALE which the losses are reduced by 33% and 30%, respectively. It can be ob-

served that the losses in the switches 5 and 8 are increased considerably, thus most of the losses of phase U are transferred to phase V. Phase W does not seem to be significantly affected by the application of the modified PWM. As it will be discussed in a further section, a tradeoff has to be found in order to obtain a beneficial result of the whole procedure.

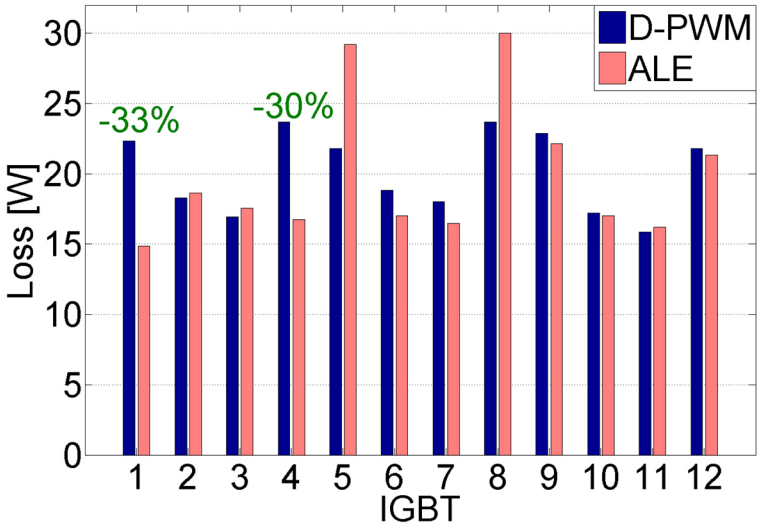


Figure 48: Losses in the 3L-NPC VSI for $m = 0.95$ and rated torque of the fed machine. Columns in blue represent the losses in D-PWM operation, in red for operation with the modified PWM

4.2.4 Optimized operation in the range of high modulation index

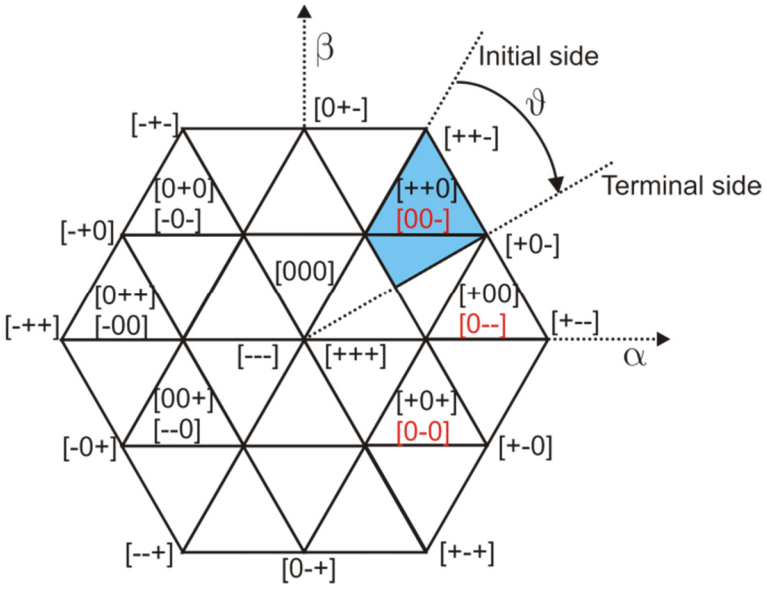
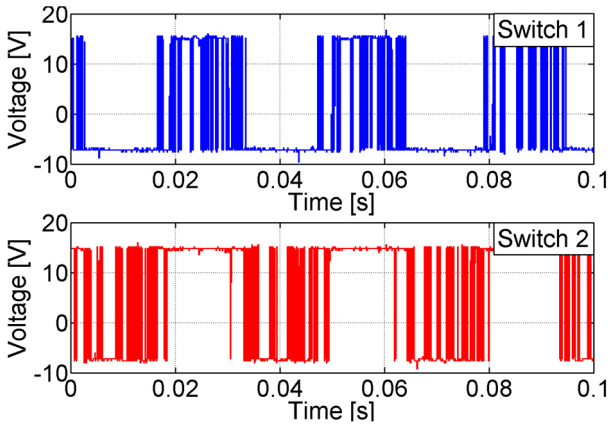


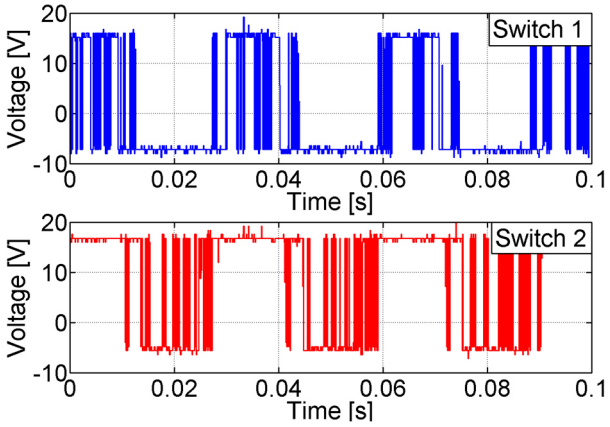
Figure 49: The modified PWM with ALE is applied in the blue sector limited by the angle ϑ

In the range of high modulation index, the modified PWM with ALE can be used for the loss reduction of the semiconductor devices by changing the control for a sector width of 120°. Such operation mode causes a large distortion on the neutral-point voltage. Yet the ripple of the neutral-point voltage can be reduced by limiting the area, in which the modulation is changed as shown in Figure 49. The angle ϑ varies within the range $0° \leq \vartheta \leq 120°$. For $\vartheta = \vartheta_{min} = 0°$, normal D-PWM is used and for $\vartheta = \vartheta_{max} = 120°$ the proposed procedure is applied in its full range, as discussed in 4.2.2.

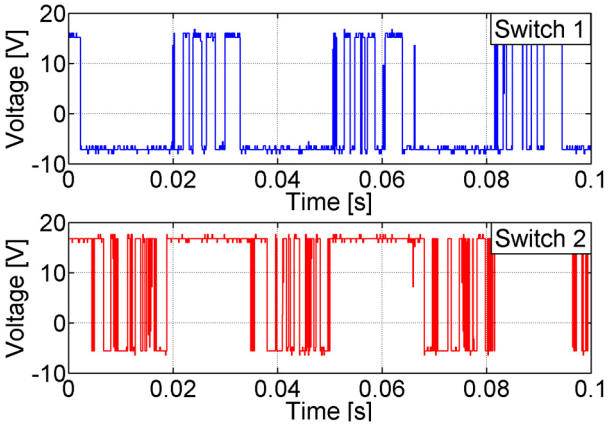
Figure 50 shows the gate signals for the switches 1 and 2 when applying the modified PWM with ALE with different reduced operational maps, which are defined with different values of the angle $\vartheta = 0°$, $\vartheta = 15°$, $\vartheta = 30°$, $\vartheta = 45°$ and $\vartheta = 120°$. In case of $\vartheta = 0°$, the inverter is operated under normal operation with the conventional D-PWM.



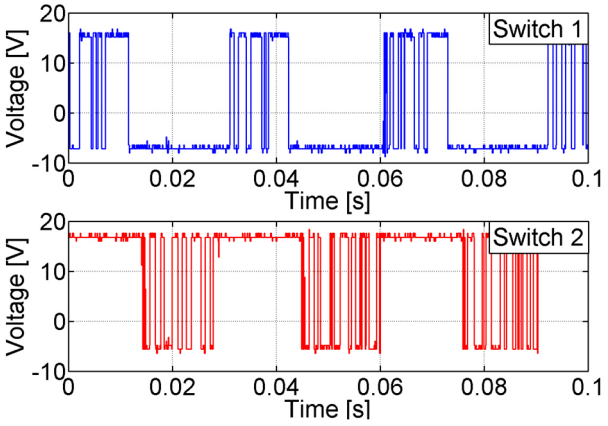
(a) Sector width $\vartheta = 0°$ (Normal D-PWM)



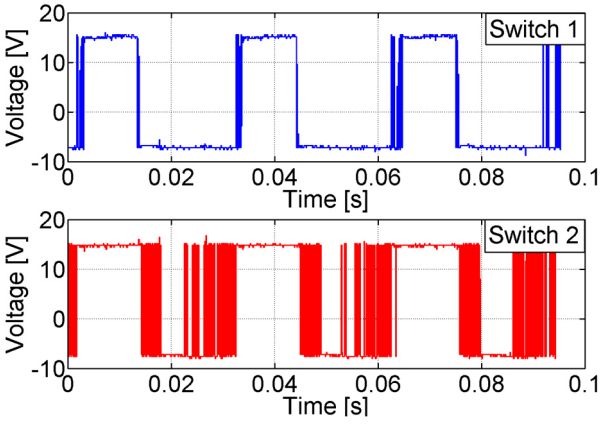
(b) Sector width $\vartheta = 15°$



(c) Sector width $\vartheta = 30°$



(d) Sector width $\vartheta = 45°$

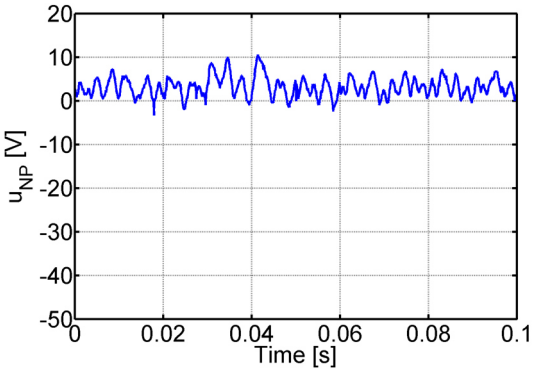


(e) Sector width $\vartheta = 120°$

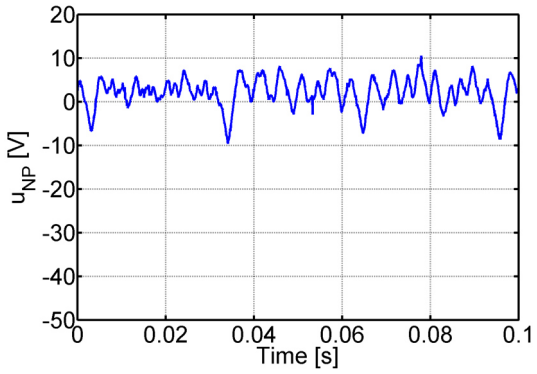
Figure 50: Gate signals for switch 1 (blue) and switch 2 (red) in case of applying modified PWM for $m = 0.68$, fundamental frequency $f_S = 32.4$ Hz and rated torque of the induction machine

Figure 51 presents the change of the neutral-point voltage ripple with respect to the increase of the angle ϑ, for same operational conditions. It shows a clear trend: the larger the value of the angle ϑ, the higher the distortion of the neutral-point voltage. Figure 51 (d) shows a large ripple of the neutral-point voltage for a clamping duration of 45°, where only the upper leg of phase U is clamped to the positive DC rail. It indicates that the use of the usual D-PWM technique, in which each leg of each phase is clamped alternatingly to the corresponding DC rail for a duration of 60 electrical degree, causes a larger distortion of the neutral-point voltage, especially for operation in the range of moderate modulation index $0.5 < m \leq 0.7$. Therefore, the D-PWM used in the recent work has been optimized, so that the clamping duration of each leg to the corresponding DC rail is varied to maintain the smallest ripple of the neutral-point voltage in the normal operation.

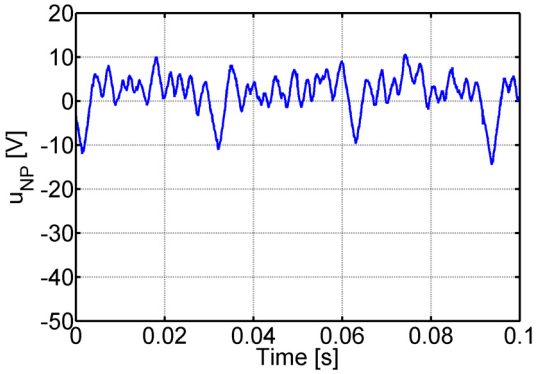
The measured load current – using different optimized operational maps and are shown in Figure 52 (a) thru Figure 52 (e).



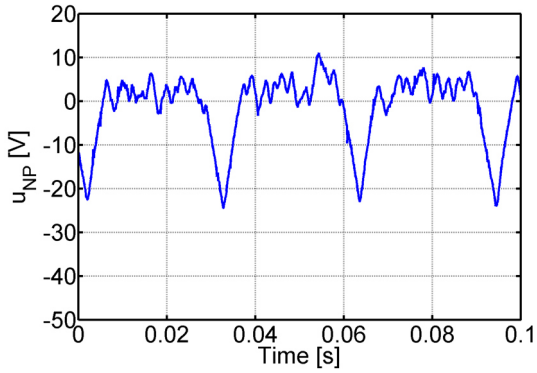
(a) Sector width $\vartheta = 0°$ (D-PWM)



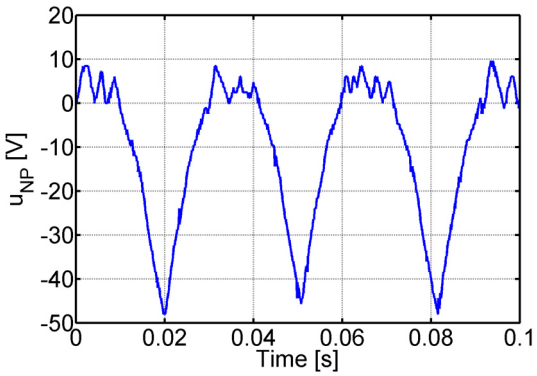
(b) Sector width $\vartheta = 15°$



(c) Sector width $\vartheta = 30°$

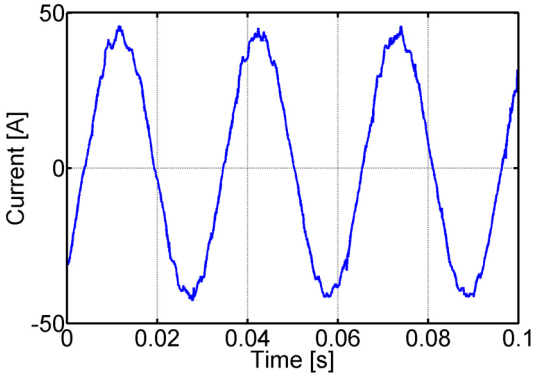


(d) Sector width $\vartheta = 45°$

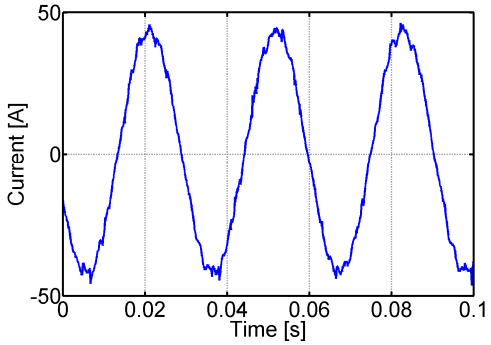


(e) Sector width $\vartheta = 120°$

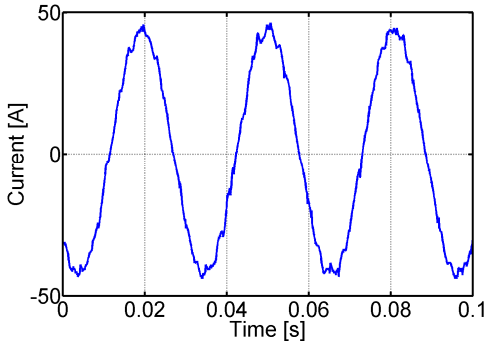
Figure 51: Neutral-point voltage for operation with a reduced sector of modified PWM with ALE, $m = 0.68$, fundamental frequency $f_S = 32.4$ Hz and rated torque of the induction machine



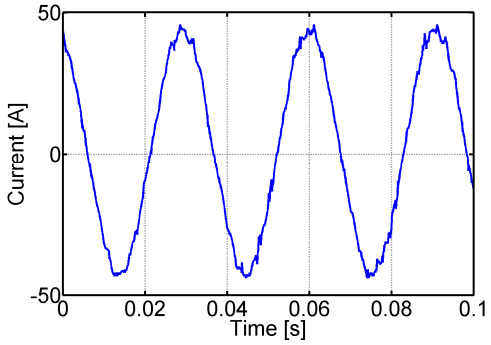
(a) Sector width $\vartheta = 0°$ (D-PWM)



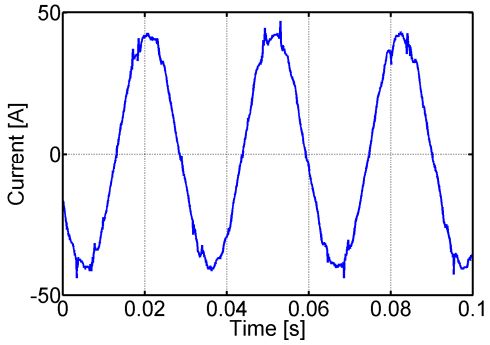
(b) Sector width $\vartheta = 15°$



(c) Sector width $\vartheta = 30°$



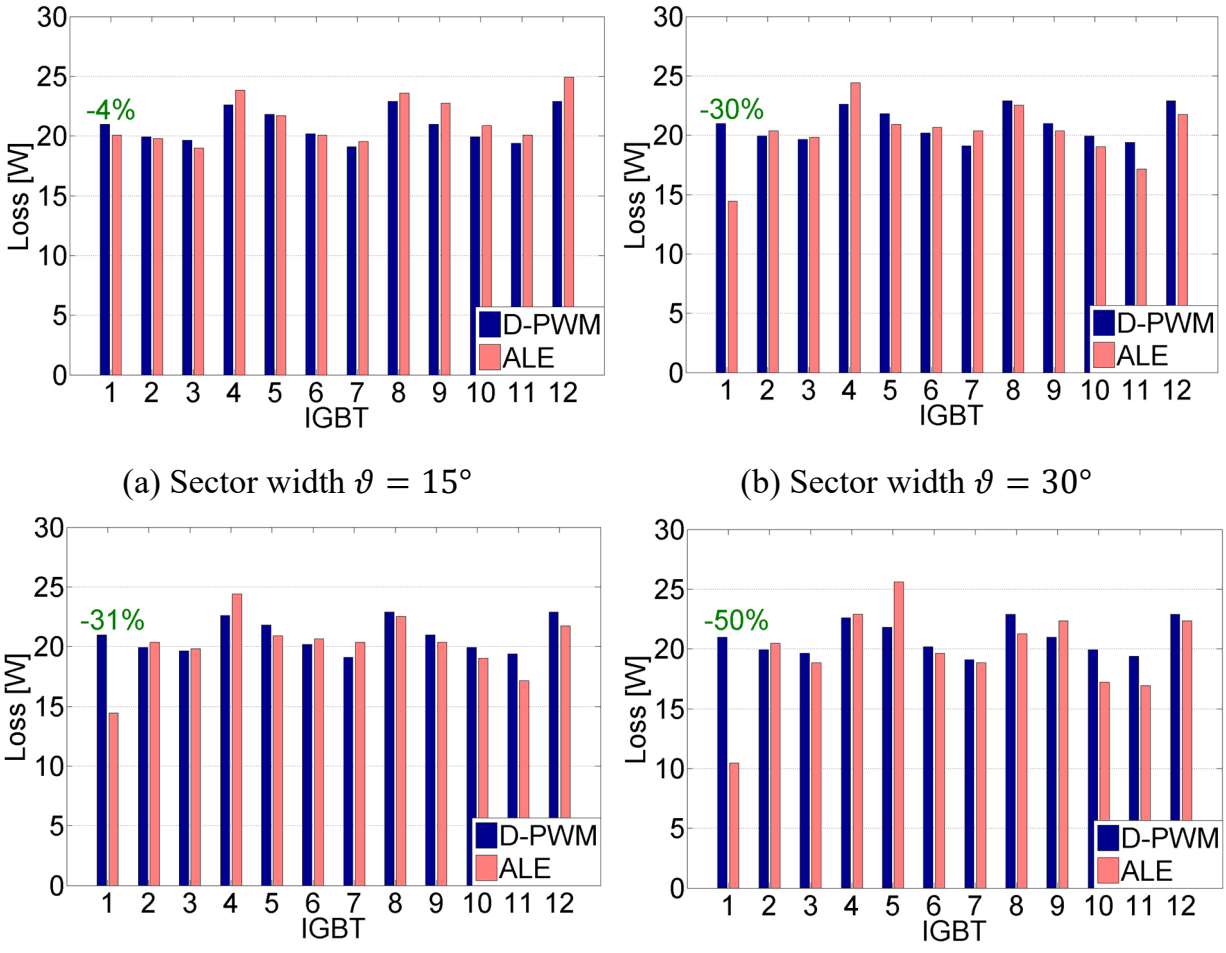
(d) Sector width $\vartheta = 45°$



(e) Sector width $\vartheta = 120°$

Figure 52: Measured load current for operation with a reduced sector of PWM with ALE, $m = 0.68$, $f_S = 32.4$ Hz and rated torque of the induction machine

Figure 53 shows the losses in the switches of the inverter, the columns in blue stand for normal D-PWM, in red for the operation with the modified PWM with ALE. In case of $\vartheta = 15°$, there is no considerable reduction of losses in switch 1. The situation changes significantly as soon as $\vartheta > 30°$, yielding at least 33% reduction of switch losses. For $\vartheta = 120°$, the highest reduction of losses can be achieved, but at the cost of excessive distortion of the neutral-point voltage. Therefore, the operation of PWM with ALE with an angle $\vartheta > 45°$ should be avoided, especially at high torque, so that the current and neutral-point voltage quality are maintained at an acceptable level.



(a) Sector width $\vartheta = 15°$

(b) Sector width $\vartheta = 30°$

(c) Sector width $\vartheta = 45°$

(d) Sector width $\vartheta = 120°$

Figure 53: Losses in the switches of the 3L-NPC VSI for m = 0.68, fundamental frequency $f_S = 32.4$ Hz and rated torque of the induction machine

4.3 Summary of the chapter

In this chapter, the performance of the proposed modified PWM scheme with ALE has been comprehensively investigated by means of measurements carried out at a dedicated laboratory set-up. The results confirm the effectiveness of the proposed PWM scheme, which has been applied successfully to redistribute the losses among the switches of the inverter in different operating points. Furthermore, the impact of the proposed modified PWM with ALE on the balancing of the neutral-point voltage was extensively investigated. Based on the obtained results, an optimum operation of the modified PWM with ALE has been developed, so that a tradeoff between the redistribution of losses and the control of the neutral-point voltage can be achieved.

5 Simulation of the system

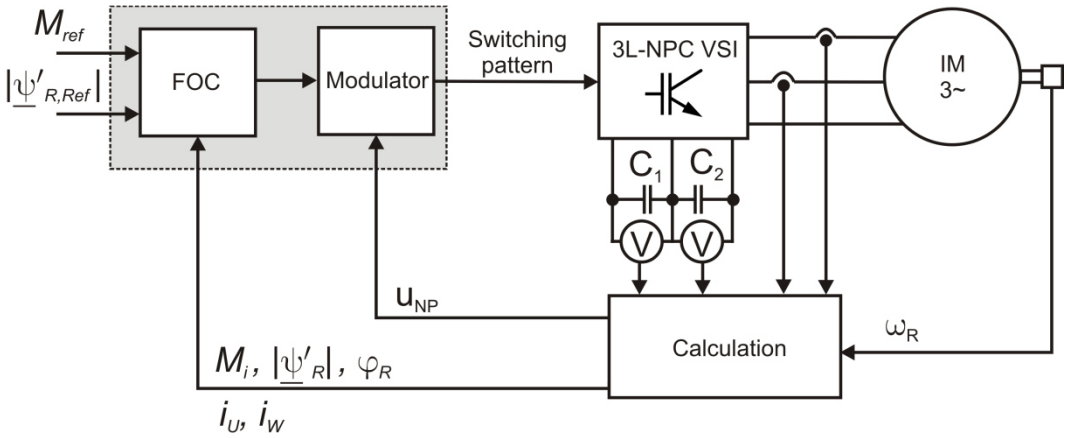


Figure 54: Overview of the simulated system

The effectiveness of the proposed control strategy has been investigated by means of experiments. The results presented in the previous chapter have shown an excellent performance in a wide range of operation. Nevertheless, the thermal measurements are a cumbersome and time-consuming procedure, due to the large value of the time constant of the heatsinks. Therefore, most of the measurements were conducted in the range of high modulation index with high load, which was considered to be the most disadvantageous range for the application of the proposed strategy and to deserve the highest attention. In contrast, the range of low modulation index offers mores degrees of freedom and the modified PWM with ALE can be applied in a straightforward way thanks to the large availability of redundancies, thus the number of measurements can be limited. In any case, a validation of the proposed PWM based only on experiments would demand numerous measurements in order to examine all effects and for its enhancement, to reduce possible negative effects in the whole operation range.

To deal with this problem, a loss model of the laboratory set-up was developed to examine the proposed modulation strategy further and to reduce the number of cumbersome and time-consuming experiments.

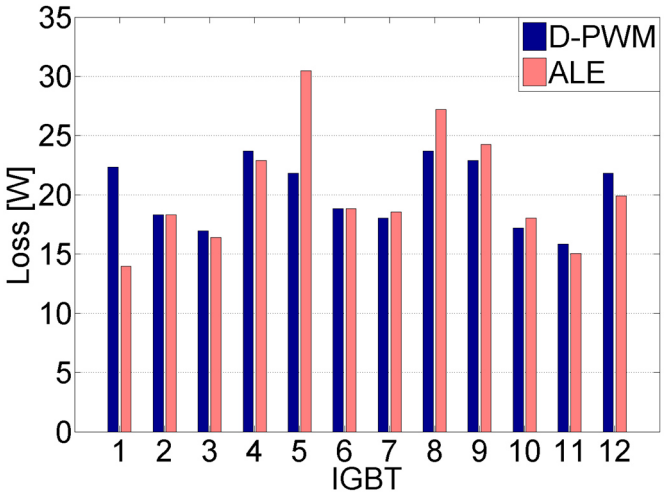
The model was implemented in Matlab/Simulink using ideal switches. Yet for the calculation of the losses each switching action was taken into account in a dedicated block. The details of the method have been discussed in 2.7, and the thermal characteristics of the examined switch are given in the annex. For the sake of simplicity, the temperature dependencies of these parameters were not taken into consideration.

The simulated structure of the electrical model of the drive consisting of inverter, electrical machine, field-oriented control and DC link is shown in Figure 54. The results obtained by the simulation of the electrical system, i.e. switching pulse pattern, current on each switch, are employed as input for the loss model. In addition, the fluctuations of the DC-link voltage were also considered for the calculation of the switching losses. The deviations from the ideal value $0.5 \cdot U_{DC}$ are especially important in the range of low modulation index, where the proposed PWM strategy causes higher ripple of the neutral-point voltage.

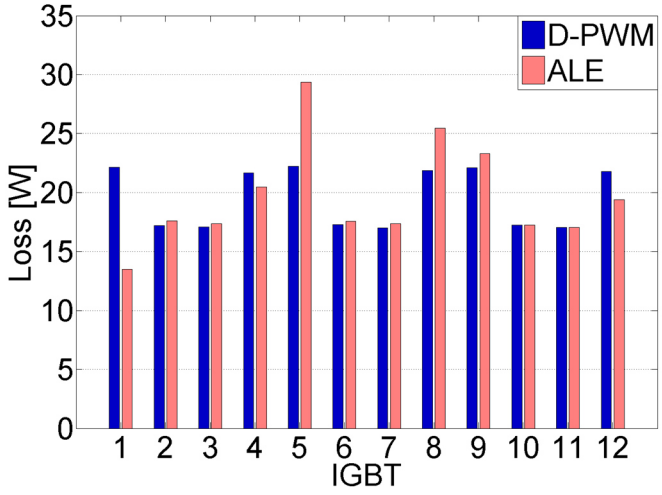
5.1 Verification of the loss model

It is well known that the losses of a semiconductor switch consist of conduction and switching losses. The conduction losses depend mostly on the voltage drop across the switch, on the load current and its power factor $cos\varphi$. The case of the switching losses is more complicated, since they do not only depend on the previously mentioned factors, but also on the design of the inverter as e.g. layout, performance of the driver circuits, choice of gate resistance, as well as on the switching frequency, etc. Therefore, the parameters of the model to estimate the conduction losses are obtained directly form the datasheet of the switch, since these are not affected by the mentioned external factors. In case of modeling switching losses, the loss-energy parameters as e.g. E_{on}, E_{off}, etc., are adapted by multiplying with a scaling factor k. This factor k was obtained by adjusting the loss model in such a way, that the values of the total losses of the switches obtained by measurement and by simulation for the same conditions have a minimal deviation. Again, the strategy is demonstrated for the reduction of losses in switch 1.

Figure 55 (a) depicts the losses in the switches as measured on the laboratory setup of the laboratory inverter for the operating point $m = 0.95$ with rated torque of the induction machine fed by the inverter. The results of the simulations in Figure 55 (b) show a good agreement with the laboratory measurement for both operating modes, operation with normal D-PWM and operation with modified PWM with ALE.



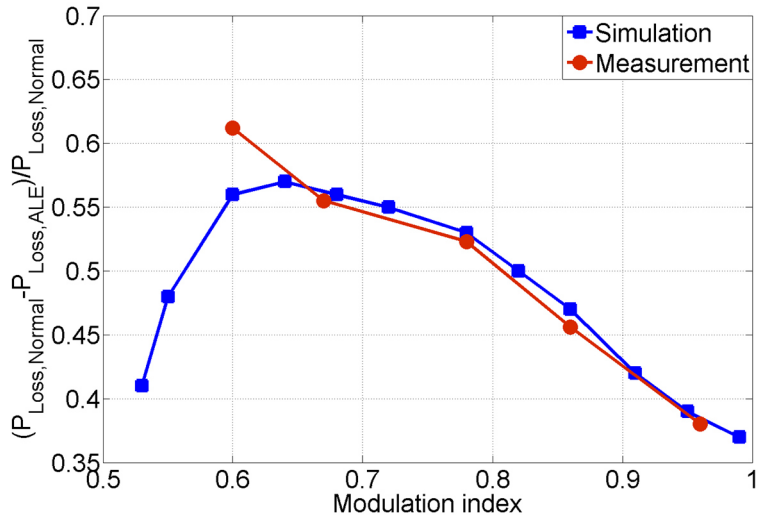
(a) Measurement



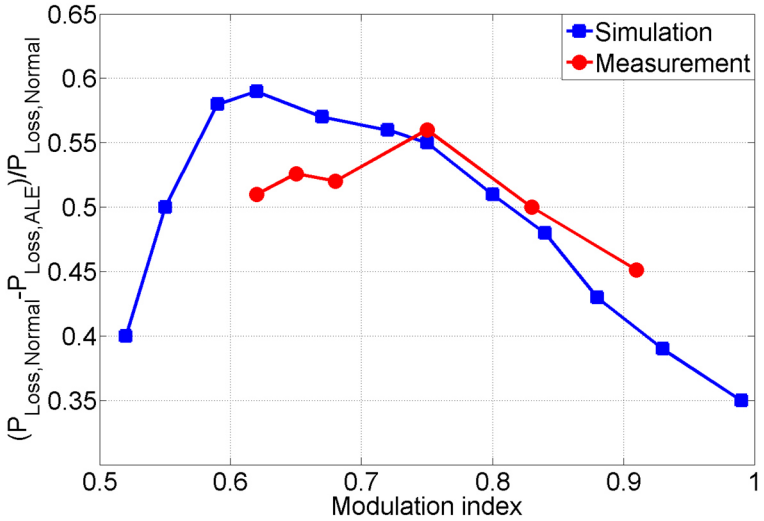
(b) Simulation

Figure 55: Total losses in the switches of the 3L-NPC VSI for $m = 0.95$ and rated torque of the machine.

Figure 56 depicts the impact of the modified PWM with ALE on the losses of switch 1 for different operating conditions, which are examined by means of measurement and simulation. The comparison presents a close agreement of the simulation results with the experimental results for various operating points.



(a) Operation with rated torque



(b) Operation with 75% rated torque

Figure 56: Reduction of losses in IGBT 1for different operating conditions

Figure 57 presents the case that delivered the maximum deviation between simulation and measurement results, being in the range of ±3 W.

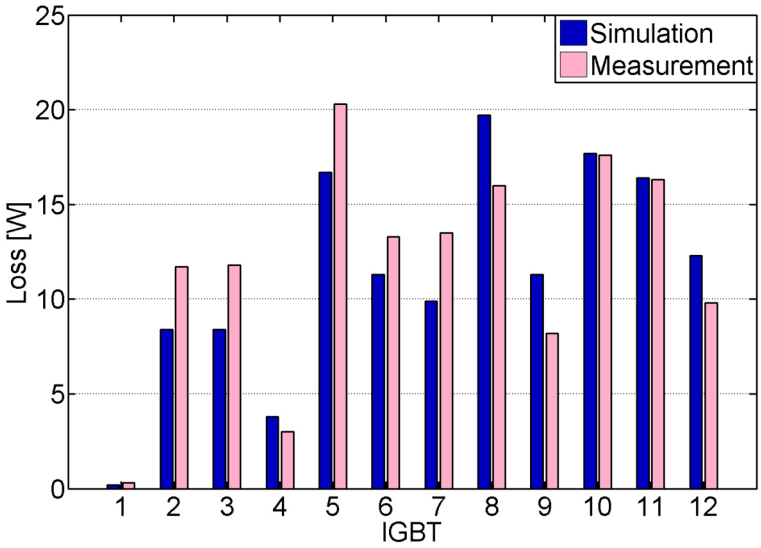


Figure 57: Comparison of losses in the switches by simulation and measurement with modified PWM with ALE for $m = 0.46$ and 40% rated torque of the induction machine

The main sources of the deviations were identified as:

- The missing consideration of temperature dependency: the loss characteristics of a switch, i.e. switching losses energy E_{on}, E_{off}, etc., are strongly dependent on the junction temperature. The consideration of these factors in the simulation requires a higher calculation effort and it is out of the scope of the recent work.
- The estimation of the losses based on the measurement of the heatsink temperature: although the measurement of the heatsink temperature by using the Pt1000 devices is considered as one of the most accurate approaches, this still has an error of ±1 K ,which results in the estimation error of the losses of ± 1 W, since the thermal resistance of the heatsink is 1.1 $\frac{\mathrm{K}}{\mathrm{W}}$. Furthermore, the value of the thermal resistance of the heatsink is not constant, since heat convection from heatsink to ambient depends strongly on heatsink temperature, ambient temperature, air turbulence, etc., as stated e.g. in [57]. In addition, the placement of the sensors is crucial, since the temperature rise of the neighbor devices causes a heating of the unit under test and

leads to systematical errors. In the course of the investigations different ideas for the improvement of the experimental set up were developed, but could not be realized due to the necessary mechanical changes and the lack of time.

- The measurement points: Since most of the measurements were conducted in the range of high modulation index, while the drive was loaded with high torque, the loss model is likely to deliver the better results in this range.

Despite of this drawback, the accuracy of the loss model is acceptable and the model can be used to investigate the effectiveness of the PWM with ALE.

5.2 Performance of PWM in range of low modulation index

Four types of operational maps for the application of PWM with ALE in the range of low modulation index have been proposed in subchapter 4.2.1. The measurements show that the use of the operational maps of type D achieves the best balance between loss reduction and control quality of the neutral-point voltage. Thus, the performance of the use of this operational map was further investigated by means of simulation.

Figure 58 depicts the reduction of losses in switch 1 for different operating points. The term $P_{Loss,Normal}$ refers to the total losses dissipated in the examined switch in normal operation with D-PWM, while $P_{Loss,ALE}$ denotes the total losses produced using PWM with ALE.

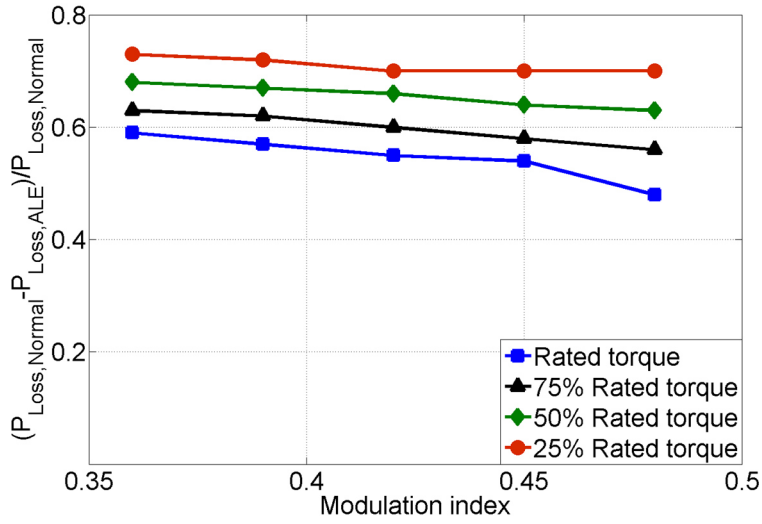


Figure 58: Change of total losses of switch 1 by applying PWM with ALE

Figure 59 shows the effect of the application of modified PWM with ALE on the losses of switch 2. The range of low modulation index is the most favorable one for the application of the proposed procedure, that can be used to reduce the losses of either switch 1 or switch 2. In contrast, only switch 1 can be relieved by applying the same scheme in the range of higher modulation.

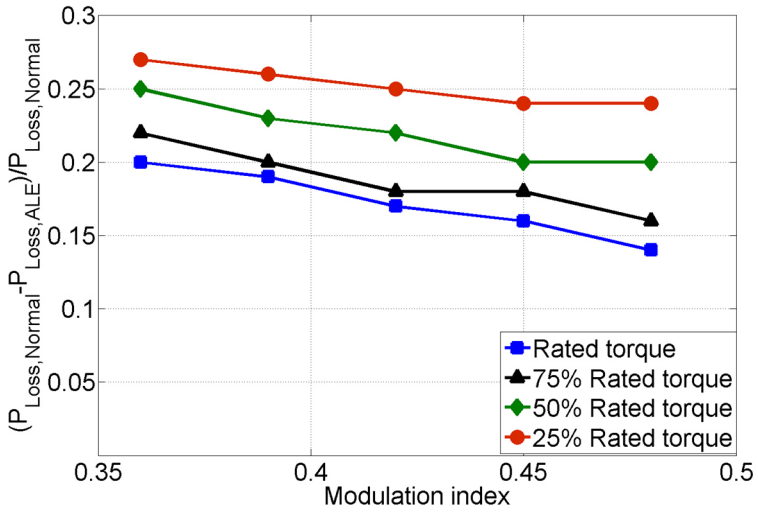


Figure 59: Change of total losses in switch 2 by applying modified PWM with ALE

Figure 60 presents the impact of the application of ALE on the control quality of the neutral-point voltage. Obviously, the ripple is increased significantly as compared to

the typical value in case of operation with the normal D-PWM technique, which is in the range of 6 V. However, the ripple is in the range $\frac{30\text{ V}}{560\text{ V}} \approx 5\%$ of the total DC-link voltage and thus acceptable in the case of fault-tolerant control mode.

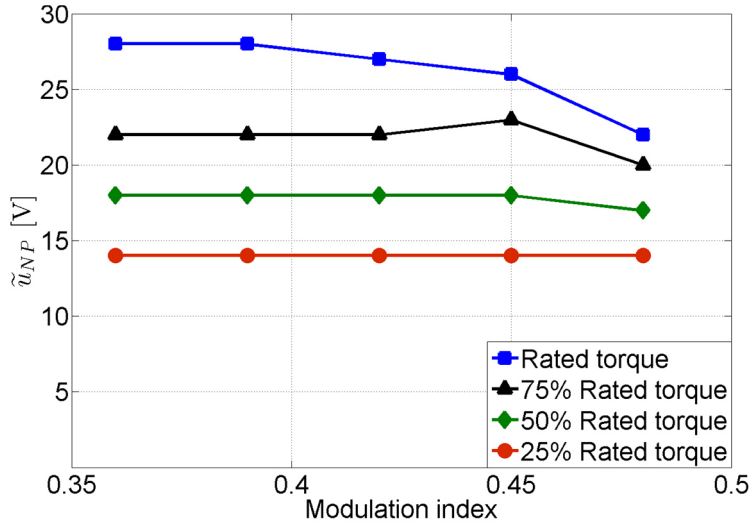


Figure 60: Ripple (peak-peak) of neutral-point voltage for operation with the modified PWM with ALE

5.3 Performance of modified PWM in the range of high modulation index

In the range of high modulation index, the modified PWM with ALE can be optimized either to reduce the switching losses or to reduce the conduction losses of the stressed switch. The impact of each approach on the total losses of the switch has been discussed in 0 3.2 and the approach aiming at the reduction of switching losses is favored for this range. Figure 61 represents the impact of this operation mode on the total losses of the examined switch 1. The application of modified PWM with ALE yields a significant reduction of total losses in the particular switch for different modulation indices and for different values of torque applied on the drive.

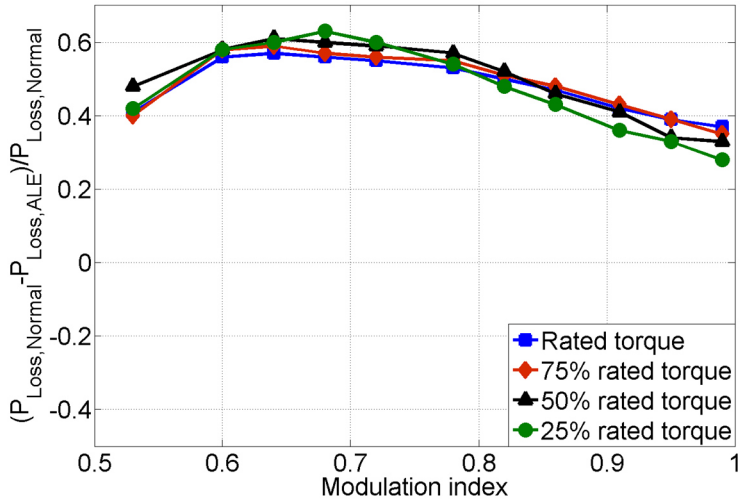


Figure 61: Change of losses of switch 1 by applying modified PWM with ALE optimized to reduce the switching losses

Figure 62 presents the performance of the proposed modulation strategy, which is optimized to reduce the conduction losses of the affected switch. Obviously, this approach increases the thermal load on the stressed switch instead of reducing and therefore the application of this approach is prohibited in this range.

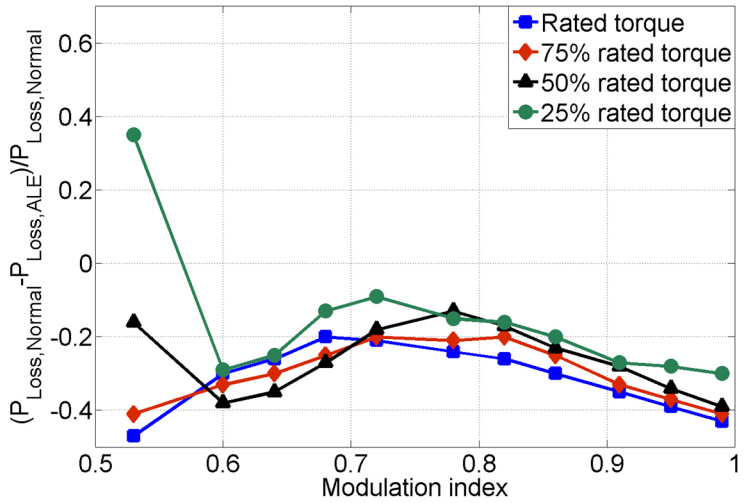


Figure 62: Change of losses of switch 1 by applying modified PWM with ALE optimized to reduce the conduction losses

5.4 Optimized operational map in range of high modulation index

In subsection 4.2.4, the improved operational map defined by the angle ϑ was shown in Figure 49. The higher the value of the angle ϑ, the more often the modified PWM with ALE can be applied to reduce the losses in the affected switch. Therefore, the amount of the reduction of losses and the distortion of the neutral-point voltage are closely associated with the choice of the value of angle ϑ.

Figure 63 shows the impact of modified PWM with ALE on the losses of switch 1 in relation to the value of the angle ϑ, where three operating points with modulation index $m = 0.99, 0.78$ and 0.60 with a load of the fed machine at rated torque are examined.

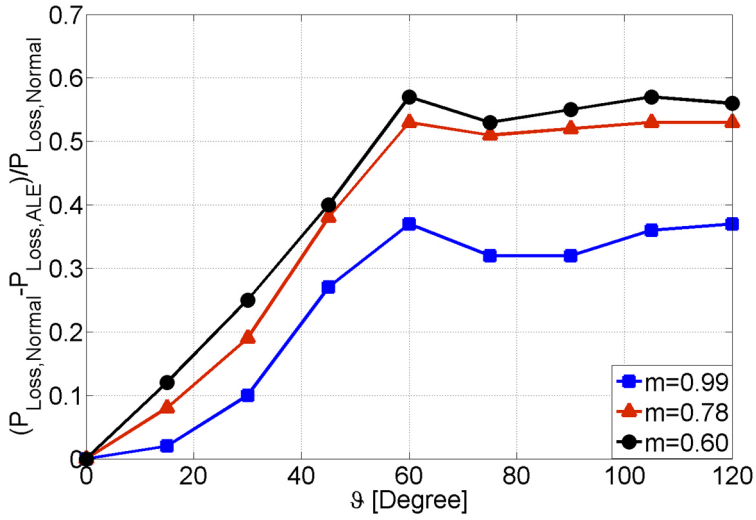


Figure 63: Change of the losses of switch 1 in dependence upon the width of the operating sector in case of operation with 100% rated torque of the fed machine and with different modulation indices

Figure 64 presents the performance of the proposed strategy in relation to the value of the angle ϑ, where the machine fed by the inverter is loaded with smaller torque, i.e. 25% of rated torque.

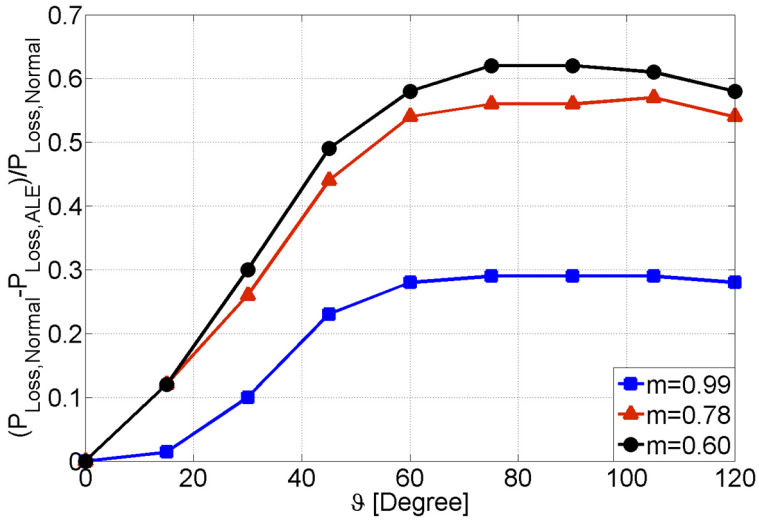


Figure 64: Change of the losses of switch 1 in dependence upon the width of the operating sector in case of operation with 25% rated torque of the fed machine and with different modulation indices

Figure 65 shows the change of the amplitude of the ripple of neutral-point voltage in relation to the value of angle ϑ in case of the drive loaded with 100% rated torque.

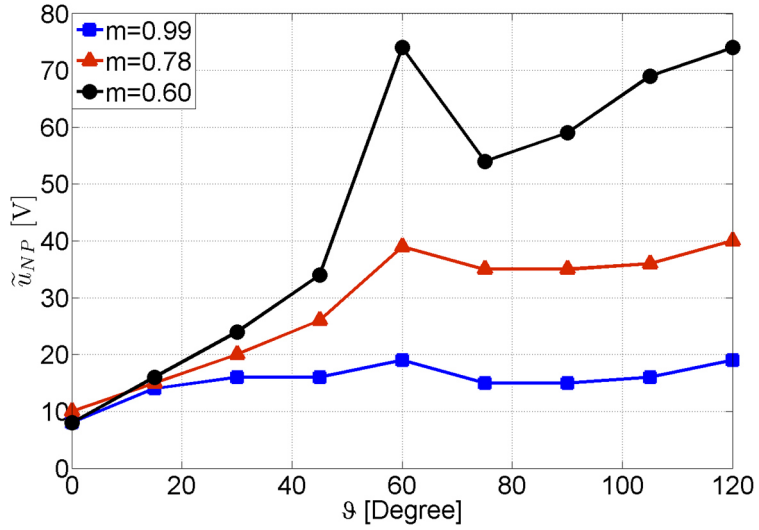


Figure 65: Ripple of neutral-point voltage (peak-to-peak) by applying the modified PWM in dependence upon the width of the operating sector. Operation with 100% rated torque on the machine fed by the inverter and different modulation indices *m*

Figure 66 shows the change of the ripple of the neutral-point voltage as a function of the value of the angle ϑ in case that the machine fed by the inverter is loaded with 25% of the rated torque. Obviously for both cases shown in Figure 65 and Figure 66, the use of the operational map defined with the angle ϑ in the range $0° \leq \vartheta \leq 45°$ yields the lower distortion of the neutral-point voltage. Therefore, this range is recommended to achieve the optimal operation of PWM with ALE.

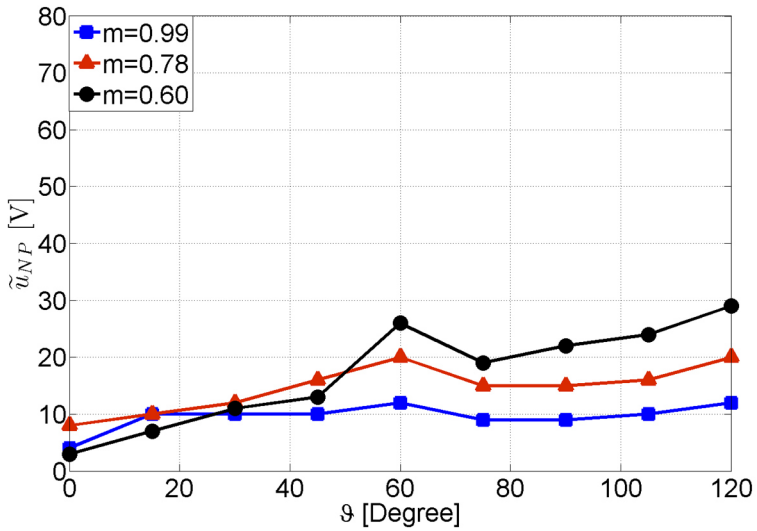


Figure 66: Ripple of neutral-point voltage (peak-to-peak) by applying the modified PWM in dependence upon the width of the operating sector. Operation with 25% of the rated torque on the machine fed by the inverter and different modulation indices

6 Direct Torque Control with ALE

The objective of this thesis is the reduction of losses in a particular overheated semiconductor device in a 3L-NPC VSI. The proposed procedure modifies the PWM in a way that the losses of an overheated device are distributed to the other switches. The solution has to take into account that the operation of the inverter should be maintained without intolerable reduction of the power and the control quality and that the negative impact on the neutral-point voltage of the DC link is minimized. In this way, under certain conditions Active Lifetime Extension for the whole system can be achieved and operation can continue until a repair is possible.

In a second step, the possible application of the same ALE for the case of DTC was examined by means of simulation and is presented in the following. Due to the limited time and to the effort of substantial changes in the control scheme the experimental validation was not carried out.

6.1 DTC for a 3L-NPC VSI

Direct Torque Control (DTC) is a well-established control method for three-phase machines and its principle was briefly described in 2.6.2. Since its introduction in the mid-1980s [20]−[22], the DTC method for two-level inverters has been continuously developed [23] and made successfully its way to the market [22]. The scheme can also be applied to multi-level inverters that offer many improvements as compared to the conventional two-level inverter: lower torque ripple, reduced switching losses, less dv/dt, reduced common-mode voltage, etc. thanks to the increase of voltage level. The three-level and five-level inverter controlled by DTC scheme are commercialized by ABB [24]−[25].

Figure 67 shows a simplified DTC scheme for an induction machine (IM) fed by a 3L-NPC VSI. The controlled variables in this scheme are the torque M_i, the magnitude of the stator-flux space vector $\left|\underline{\psi}_s\right|$ and the neutral-point voltage of the inverter u_{NP}.

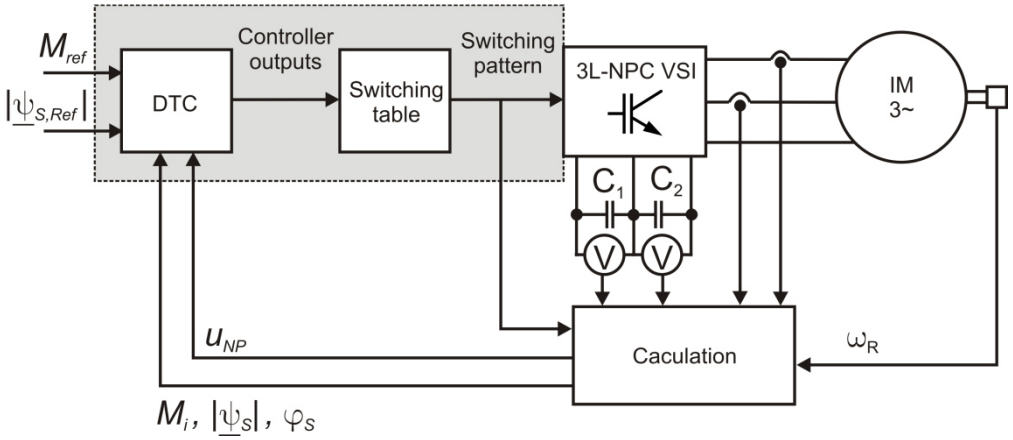


Figure 67: Principal scheme of DTC for an 3L-NPC VSI feeding an induction machine using a switching table

The actual values of torque M_i and of magnitude of the stator flux $\left|\underline{\psi}_s\right|$ are computed based on the measured phase currents, on the switching pattern and on the measured DC-link voltage. The actual values of the controlled variables are compared with their reference values by hysteresis controllers. The choice of the proper voltage space vector is based on the values of hysteresis controller outputs and on the actual location of the stator-flux space vector $\underline{\psi}_s$. Furthermore, a look-up table considering the influence of each voltage space vector on the stator-flux space vector has to be used for making the appropriate choice. If the optimum voltage space vector applied to the inverter is a short one, e.g. space vectors $15[-0-]/21[0+0]$ (see Figure 68), an additional degree of freedom is provided to control the neutral-point voltage. Here, the selection of the appropriate redundant switching states of a short voltage space vector is based on the output of the neutral-point voltage controller and on the sign of the total current flowing into the neutral point.

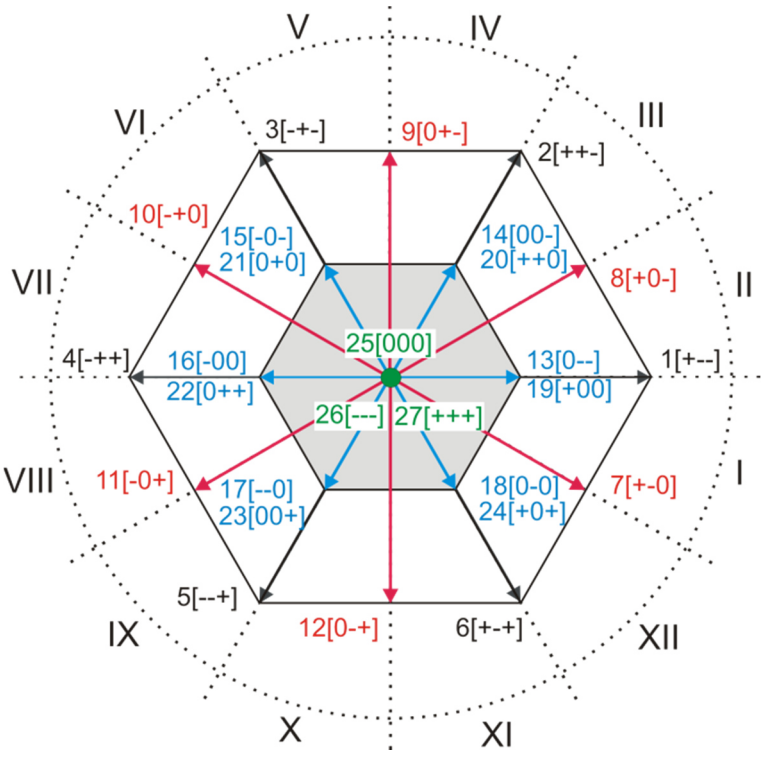


Figure 68: Partition of space-vector diagram into 12 sections. The vectors in black/red/blue/green refer to long/medium/short/zero voltage space vectors.

The look-up table of the DTC scheme for the 3L-NPC VSI is shown in Table 6-I. The three first columns of the table correspond to the outputs of the hysteresis controllers for each controlled variable: flux (*OutF*), torque (*OutT*) and neutral-point voltage (*OutNP*), respectively. SignI is the sign of the total current flowing into the neutral point of the DC link and the assignment of SignI for each short voltage space vector will be shown. The sectors I to XII correspond to the location of the flux space vector $\underline{\psi}_s$ at the sampling instant. If the torque error is large, the medium or long voltage space vectors spanning the outer hexagon are used to control the inverter. Since these do not have any redundant states, the output of the neutral-point voltage controller cannot be taken into consideration by the selection of the switching state. Thus, the notation “x” of the third column stands for “do-not-care” state.

OutF	OutT	OutNP *SignI	Sector											
			I	II	III	IV	V	VI	VII	VIII	IX	X	XI	XII
+2	+2	x	2	9	3	10	4	11	5	12	6	7	1	8
	+1	+1	20	20	15	15	22	22	17	17	24	24	13	13
		-1	14	14	21	21	16	16	23	23	18	18	19	19
	0	+1	13	13	20	20	15	15	22	22	17	17	24	24
		-1	19	19	14	14	21	21	16	16	23	23	18	18
	-1	+1	24	24	13	13	20	20	15	15	22	22	17	17
		-1	18	18	19	19	14	14	21	21	16	16	23	23
	-2	x	12	6	7	1	8	2	9	3	10	4	11	5
+1	+2	x	2	9	3	10	4	11	5	12	6	7	1	8
	+1	+1	20	20	15	15	22	22	17	17	24	24	13	13
		-1	14	14	21	21	16	16	23	23	18	18	19	19
	0	+1	25											
		-1												
	-1	+1	24	24	13	13	20	20	15	15	22	22	17	17
		-1	18	18	19	19	14	14	21	21	16	16	23	23
	-2	x	12	6	7	1	8	2	9	3	10	4	11	5
-1	+2	x	9	3	10	4	11	5	12	6	7	1	8	2
	+1	+1	15	15	22	22	17	17	24	24	13	13	20	20
		-1	21	21	16	16	23	23	18	18	19	19	14	14
	0	+1	25											
		-1												
	-1	+1	17	17	24	24	13	13	20	20	15	15	22	22
		-1	23	23	18	18	19	19	14	14	21	21	16	16
	-2	x	5	12	6	7	1	8	2	9	3	10	4	11
-2	+2	x	9	3	10	4	11	5	12	6	7	1	8	2
	+1	+1	15	15	22	22	17	17	24	24	13	13	20	20
		-1	21	21	16	16	23	23	18	18	19	19	14	14
	0	+1	22	22	17	17	24	24	13	13	20	20	15	15
		-1	16	16	23	23	18	18	19	19	14	14	21	21
	-1	+1	17	17	24	24	13	13	20	20	15	15	22	22
		-1	23	23	18	18	19	19	14	14	21	21	16	16
	-2	x	5	12	6	7	1	8	2	9	3	10	4	11

Table 6-I Switching table for DTC of 3L-NPC VSI, notation “x” denotes “ignore” state.

The design of the hysteresis controllers of the DTC scheme for multi-level voltage source inverters can be derived from that used for two-level inverters by considering the additional output voltage levels as shown in [23], [25]. There, for an *n*-level inverter, the torque controller has a characteristic that comprises $(2n-2)$ hysteresis bands, to deliver $(2n-1)$ discrete output values. Here, the control of torque has the higher priority than the control of flux and neutral-point voltage. Figure 69 shows the characteristic of the torque controller for the 3L-NPC VSI used in this work. By choosing$n=$

3, the outputs $OutT = [-2;\ -1;\ 0;\ +1;\ +2]$ are defined and correspond to the second column in Table 6-I. The thresholds H_{T1} and H_{T2} determine the width of the hysteresis band of the torque and are set based on empirical and calculated values. For the value $|OutT| = 2$, the long and medium voltage space vectors are applied. The use of *medium-voltage* space vectors causes disturbance of the control of neutral-point voltage, since one of the three phases of the inverter is connected to the neutral point. An improvement of neutral-point voltage control can be achieved by avoiding the use of medium voltage space vectors, but at the expense of higher switching losses and lower current quality, which in practice is not accepted. In case of $|OutT| = 1$, short voltage space vectors are employed and their redundancies can be also used, either to control the neutral-point voltage or to redistribute the losses. In the case of $OutT = 0$, the zero space vector is used and only the switching state 25[000] is applied to control the inverter.

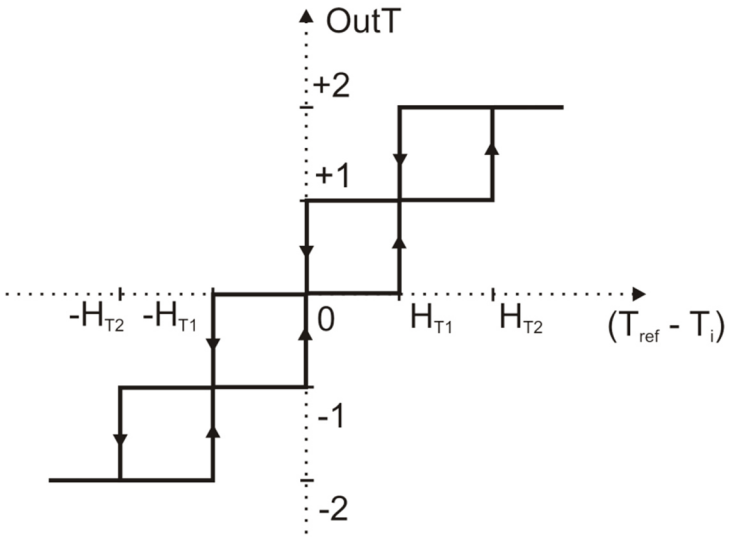


Figure 69: Characteristic of the 5-level hysteresis torque controller

The switching states 26[− − −] and 27[+ + +] are not utilized, in order to reduce the switching-losses of the inverter. For the values $|OutT| = 2$ or $OutT = 0$, the short

voltage space vectors are not employed, thus the control of the neutral-point voltage is not possible.

In principle, the flux controller could take the same structure as in a DTC scheme for a two-level inverter, in which the flux controller has the two outputs $[-1; +1]$. However if the same characteristic is used, the control quality of the flux becomes poor in the case that the torque control output $OutT = 0$, in which the zero voltage space vector is used. To enhance the function of the flux controller, its characteristic is extended with two additional outputs $[-2; +2]$. In this way, the short voltage space vectors are used in the case of $OutT = 0$, if the stator-flux error become too large. The control quality of the neutral-point voltage is also improved with this modification, since the use of short voltage space vectors is increased. The characteristic of the flux controller is shown in Figure 70, here the thresholds H_{F1} and H_{F2} determine the width of the hysteresis band for the amplitude of the stator-flux space vector.

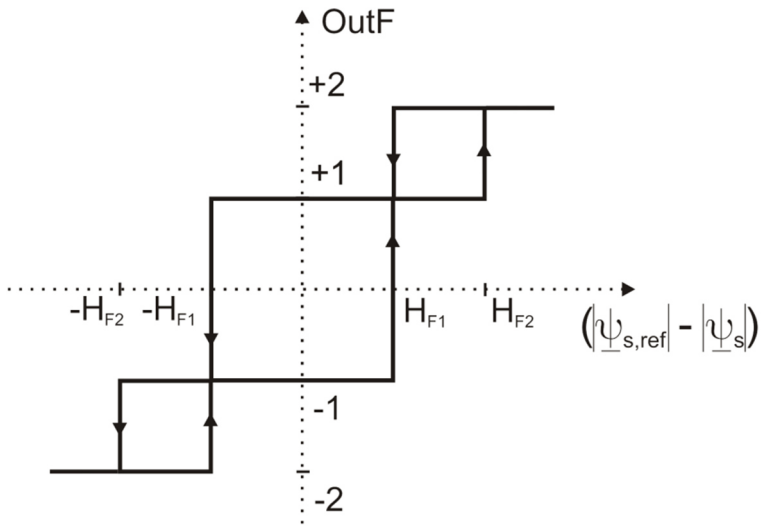


Figure 70: Characteristic of the 4-level hysteresis flux controller

Figure 71 depicts the characteristic of the 3-level hysteresis controller for the neutral-point voltage. The output can take in the values $OutNP = [-1; 0; +1]$. The thresholds H_{NP1} and H_{NP2} determine the ripple of the neutral-point voltage. For the values $OutNP = [-1; +1]$ the redundancies of the space vectors can and have to be taken into account by the generation of switching pattern. For this control purpose, the prod-

uct $OutNP \cdot SignI$ is used and is assigned in the third column of Table 6-I, where *SignI* is the sign of the total current flowing into the neutral point of the DC link. The assignment of *SignI* for each short voltage space vector is shown in Table 6-II.

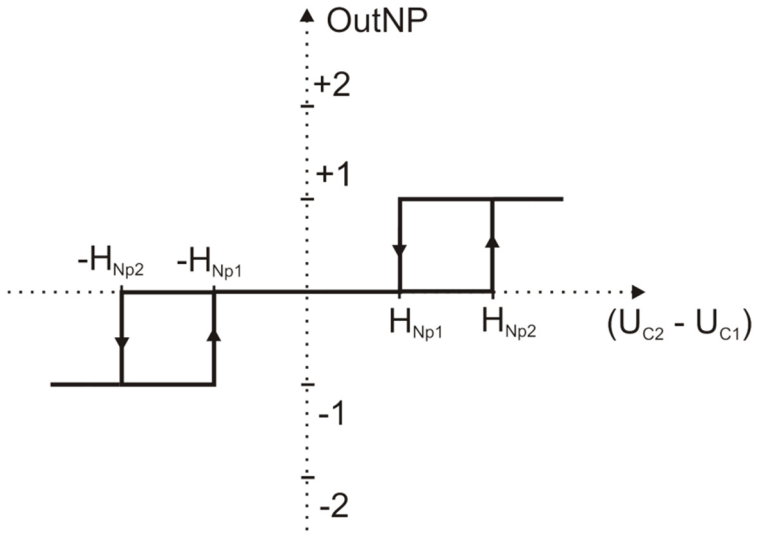


Figure 71: Characteristic of the 3-level hysteresis neutral-point voltage controller

The redundant switching states can be classified into two groups according to their impact on the neutral-point voltage. For example regarding the pair $13[0--]$ /$19[+00]$ that delivers the same line-to-line voltage output, the switching state $13[0--]$ connects the phase U to the neutral point or $i_{NP} = i_U$, and is named as *non-inverse state*. In contrast, the state $19[+00]$ injects into the neutral point a total neutral-point current of $i_{NP} = i_V + i_W = -i_U$, therefore it is called as *inverse state*. The switching states $13[0--]$, $15[-0-]$, $17[--0]$, $20[++0]$, $22[0++]$ and $24[+0+]$ are *non-inverse redundant states*, which are characterized by connecting one phase to the neutral point. Conversely, the switching states $14[00-]$, $16[-00]$, $18[0-0]$, $19[+00]$, $21[0+0]$ and $23[00+]$ are *inverse redundant states*, which are characterized by connecting two output phases to the neutral point. The product $OutNP \cdot SignI$ in the third column of Table 6-I is required for the choice of the proper redundant state of a particular short space vector due to the equation (47)

$$OutNP \cdot SignI = \begin{cases} 1 & use\ the\ non-inverse\ redundant\ state \\ -1 & use\ the\ inverse\ redundant\ state. \end{cases} \quad (47)$$

If the product $OutNP \cdot SignI = 0$, a switching among the redundant switching states is not necessary. The assignment of SignI for each short voltage space vector is shown in Table 6-II.

Redundant switching states	SignI
13[**0** − −]/19[+**00**] 16[−**00**]/22[**0** + +]	$\boldsymbol{sign(I_U)}$
15[−**0**−]/21[0+0] 18[**0** − **0**]/24[+**0**+]	$\boldsymbol{sign(I_V)}$
14[**00**−]/20[+ + **0**] 17[− − **0**]/23[**00**+]	$\boldsymbol{sign(I_W)}$

Table 6-II Consideration of the sign of the phase current for the control of the neutral-point voltage

6.2 A modified DTC switching table with ALE

As mentioned above, the short voltage space vectors in the vertices of the shaded hexagon in Table 6-I are redundant, e.g. the pair 18[0 − 0]/24[+0+]. For the control of the torque as well as of the stator flux it is irrelevant, if the switching states e.g. 18[0 − 0] or 24[+0+] are used. However, their impact on the neutral-point voltage and on the loss distribution among the switches of the inverter is significant (see 2.1). Usually the redundancies of short voltage space vectors are employed for the control of the neutral-point voltage, which was reported widely in literature [31] thru [34], [41] thru [46]. In the following, the strategy for the use of the redundant states to redistribute the losses among the switches of the 3L-NPC VSI will be presented. It is assumed that the switches 1 and 2 in Figure 18 are exposed to excess of thermal load and have to be relieved to avoid the thermal breakdown.

From the knowledge of the application of the ALE strategy for the space-vector modulation (SV-PWM) as described in the previous chapters, two approaches are known:

- **Approach 1:** the redundant switching states can be used to reduce the conduction losses of IGBTs 1 and 2 at the cost of higher switching losses for the same switches

- **Approach 2:** the opposite one of approach 1, which aims at the reduction of switching losses at the cost of increasing the conduction losses at the same switches.

Table 6-I shows the switching table of a conventional DTC scheme for the 3L-NPC VSI. The highlighted fields refer to the switching states that affect the loss creation in switches 1 and 2, where the highlighted ones in *blue* are the non-redundant voltage space vectors. In contrast, the ones in green are redundant, which can be used to redistribute the losses from switches 1 and 2 to the other switching devices. Due to the distribution of the switching states in green, the ALE strategy is applicable to all 12 sectors. This seems to be more favorable in a DTC scheme than in the case of SV-PWM, in which the fault tolerant procedure can only be applied in a certain limited region of the space-vector diagram.

In the following, both *approach 1 (reduction of conduction losses)* and *approach 2 (reduction of switching losses)* will be examined. According to the targets of approach 1 or of approach 2 (see chapter 0), those switching states that are adverse to their intended achievement have to be excluded from the consideration. In both cases the switching table can be modified in the sectors VII – XII in such a way that the inappropriate switching states are replaced by their redundant states, in order to reduce the losses of the affected devices. As expected, such manipulation leads to deteriorating control quality of the neutral-point voltage, which has been already observed in case of application of SV-PWM with ALE.

6.2.1 Modification of DTC switching table by approach 1

Strategy: *Approach 1 (reduction of conduction losses)* is applied to the *sectors VII* to *sectors XII*, in which the switching states 19[+00], 20[+ + 0], 24[+0+] are replaced by switching states 13[0 − −], 14[00−] and 18[0 − 0], respectively. The modified fields of the switching table are highlighted in red. The assignment of *SignI* for each short voltage space vector is shown in Table 6-II.

OutF	OutT	OutNP *SignI	Sector											
			I	II	III	IV	V	VI	VII	VIII	IX	X	XI	XII
+2	+2	x	2	9	3	10	4	11	5	12	6	7	1	8
	+1	+1	20	20	15	15	22	22	17	17	18	18	13	13
		-1	14	14	21	21	16	16	23	23	18	18	13	13
	0	+1	13	13	20	20	15	15	22	22	17	17	18	18
		-1	19	19	14	14	21	21	16	16	23	23	18	18
	-1	+1	24	24	13	13	20	20	15	15	22	22	17	17
		-1	18	18	19	19	14	14	21	21	16	16	23	23
	-2	x	12	6	7	1	8	2	9	3	10	4	11	5
+1	+2	x	2	9	3	10	4	11	5	12	6	7	1	8
	+1	+1	20	20	15	15	22	22	17	17	18	18	13	13
		-1	14	14	21	21	16	16	23	23	18	18	13	13
	0	+1	25											
		-1												
	-1	+1	24	24	13	13	20	20	15	15	22	22	17	17
		-1	18	18	19	19	14	14	21	21	16	16	23	23
	-2	x	12	6	7	1	8	2	9	3	10	4	11	5
-1	+2	x	9	3	10	4	11	5	12	6	7	1	8	2
	+1	+1	15	15	22	22	17	17	18	18	13	13	14	14
		-1	21	21	16	16	23	23	18	18	13	13	14	14
	0	+1	25											
		-1												
	-1	+1	17	17	24	24	13	13	14	14	15	15	22	22
		-1	23	23	18	18	19	19	14	14	21	21	16	16
	-2	x	5	12	6	7	1	8	2	9	3	10	4	11
-2	+2	x	9	3	10	4	11	5	12	6	7	1	8	2
	+1	+1	15	15	22	22	17	17	18	18	13	13	14	14
		-1	21	21	16	16	23	23	18	18	13	13	14	14
	0	+1	22	22	17	17	24	24	13	13	14	14	15	15
		-1	16	16	23	23	18	18	13	13	14	14	21	21
	-1	+1	17	17	24	24	13	13	14	14	15	15	22	22
		-1	23	23	18	18	19	19	14	14	21	21	16	16
	-2	x	5	12	6	7	1	8	2	9	3	10	4	11

Table 6-III Switching table for approach 1; the substitutions are marked in red.

6.2.2 Modification of DTC switching table by approach 2

Strategy: *Approach 2 (reduction of switching losses)* is examined for *sectors VII* to *sectors XII*, in which the switching states $13[0--]$, $14[00-]$ and $18[0-0]$ are replaced by switching states $19[+00]$, $20[++0]$, $24[+0+]$, respectively. The modified fields of the switching table are highlighted in red. The assignment of *SignI* for each short voltage space vector is shown in Table 6-II.

OutF	OutT	OutNP *SignI	Sector											
			I	II	III	IV	V	VI	VII	VIII	IX	X	XI	XII
+2	+2	x	2	9	3	10	4	11	5	12	6	7	1	8
	+1	+1	20	20	15	15	22	22	17	17	24	24	19	19
		-1	14	14	21	21	16	16	23	23	24	24	19	19
	0	+1	13	13	20	20	15	15	22	22	17	17	24	24
		-1	19	19	14	14	21	21	16	16	23	23	24	24
	-1	+1	24	24	13	13	20	20	15	15	22	22	17	17
		-1	18	18	19	19	14	14	21	21	16	16	23	23
	-2	x	12	6	7	1	8	2	9	3	10	4	11	5
+1	+2	x	2	9	3	10	4	11	5	12	6	7	1	8
	+1	+1	20	20	15	15	22	22	17	17	24	24	19	19
		-1	14	14	21	21	16	16	23	23	24	24	19	19
	0	+1	25											
		-1												
	-1	+1	24	24	13	13	20	20	15	15	22	22	17	17
		-1	18	18	19	19	14	14	21	21	16	16	23	23
	-2	x	12	6	7	1	8	2	9	3	10	4	11	5
-1	+2	x	9	3	10	4	11	5	12	6	7	1	8	2
	+1	+1	15	15	22	22	17	17	24	24	19	19	20	20
		-1	21	21	16	16	23	23	24	24	19	19	20	20
	0	+1	25											
		-1												
	-1	+1	17	17	24	24	13	13	20	20	15	15	22	22
		-1	23	23	18	18	19	19	20	20	21	21	16	16
	-2	x	5	12	6	7	1	8	2	9	3	10	4	11
-2	+2	x	9	3	10	4	11	5	12	6	7	1	8	2
	+1	+1	15	15	22	22	17	17	24	24	19	19	20	20
		-1	21	21	16	16	23	23	24	24	19	19	20	20
	0	+1	22	22	17	17	24	24	19	19	20	20	15	15
		-1	16	16	23	23	18	18	19	19	20	20	21	21
	-1	+1	17	17	24	24	13	13	20	20	15	15	22	22
		-1	23	23	18	18	19	19	20	20	21	21	16	16
	-2	x	5	12	6	7	1	8	2	9	3	10	4	11

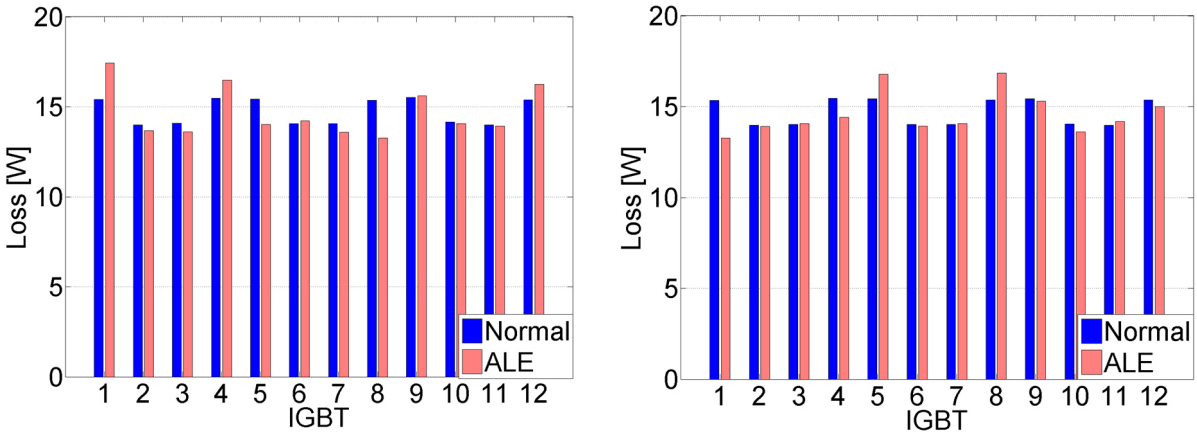
Table 6-IV Switching table for approach 2; the substitutions are marked in red.

6.3 Results of simulations

As explained above, the experimental validation of the proposed DTC with ALE was not feasible and therefore only a simulation of the system was performed. Since many simulation results had been corroborated by measurements previously, its degree of confidence is acceptable for confirming the principal validity of the proposed procedure.

The laboratory set-up as described in 4.1 with the parameters as in 9.1 was simulated to investigate the impact of the proposed ALE strategy on the performance of the inverter.

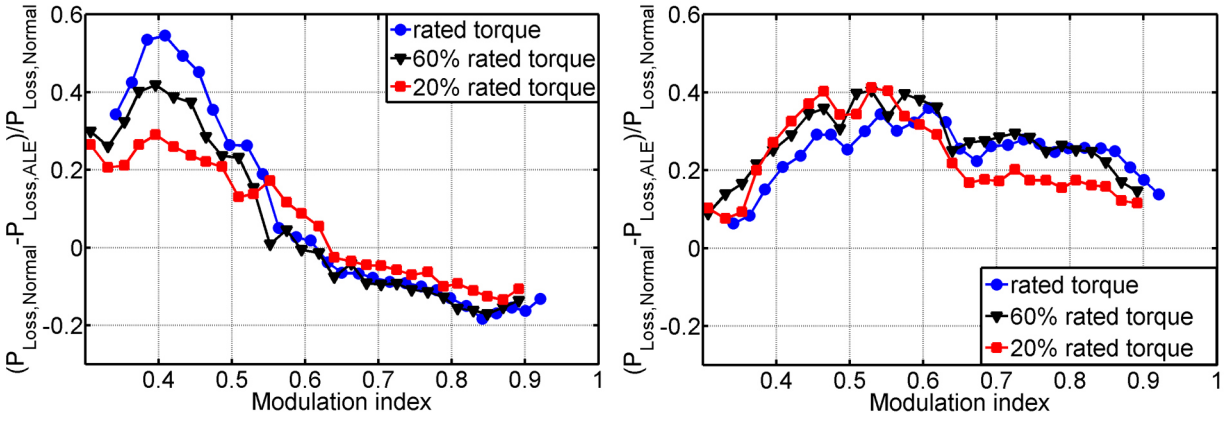
Figure 72 shows the losses in the switches of the 3L-NPC-VSI in case of $m = 0.92$ and rated torque of the machine fed by the inverter. The columns in the colors red or blue present the total losses of each mode of operation DTC with ALE and normal DTC operation, respectively.



(a) Approach 1 (b) Approach 2

Figure 72 Losses in the switches of the inverter for $m = 0.92$ and rated torque of the fed induction machine

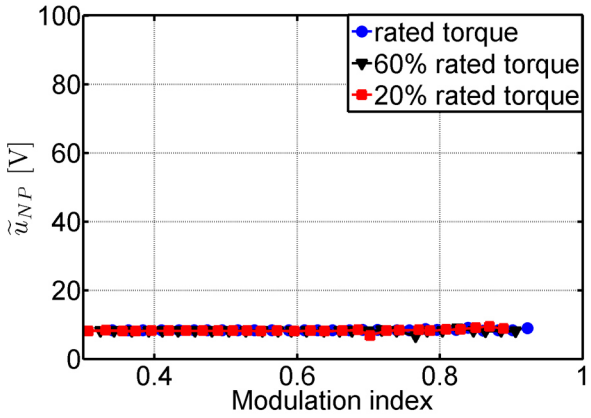
Figure 73 shows the reduction of losses in switch 1 as a function of the modulation index and for different values of the load of the induction machine fed by the inverter. For the sake of comparison the modulation index is defined as in (43) (subchapter 3.1), by taking for U_{LL} the fundamental of the line-to-line voltage as it results from the simulation. $P_{Loss,Normal}$ refers to the total losses of switch 1 in normal operation with the original switching table. $P_{Loss,ALE}$ refers to the total losses of switch 1 in DTC with ALE operation with the modified switching table. Negative values indicate higher losses, thus the modified switching table is counterproductive and the ALE strategy should not be applied.



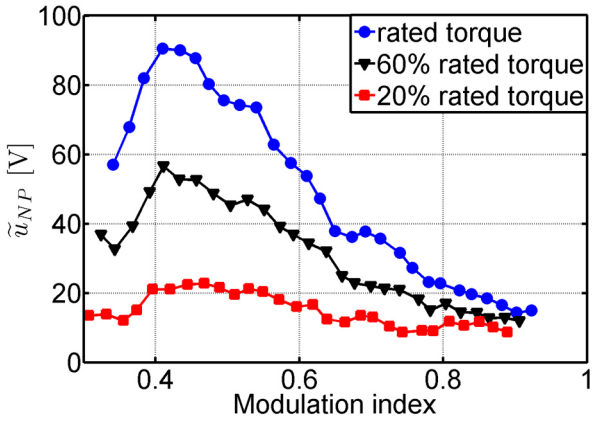
(a) Approach 1 (b) Approach 2

Figure 73 Reduction of losses in switch 1

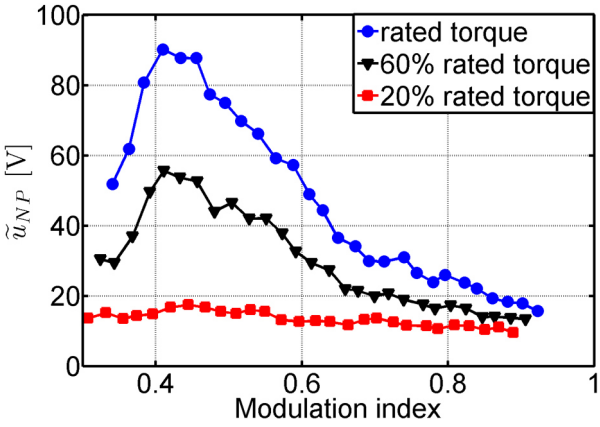
Figure 74 depicts the neutral-point voltage imbalance for different operation modes. Obviously, the ripple is increased significantly as compared to the value in case of operation with the conventional DTC scheme.



(a) Normal operation



(b) Approach 1



(c) Approach 2

Figure 74: Ripple of the neutral-point voltage (peak-to-peak value)

7 Active Lifetime Extension

7.1 Failures of IGBTs

Due to the increasing energy cost, a high efficiency of voltage source inverters (VSI) is a key requirement in industry applications. In addition, the improvement of reliability of VSI becomes more and more important for the users, since it has a high impact on the total life-cycle cost (LCC) of the system. Many VSIs are equipped with Insulated Gate Bipolar Transistors (IGBTs), due to their good switching characteristics and their high efficiency. Although IGBTs are rugged, they still suffer from failures due to excessive thermal and electrical stress, among other factors. Therefore, IGBTs can be considered as one of the lifetime-critical components of the VSIs. The failures of IGBTs [61] may be categorized in three groups:

- **Open-circuit faults**: these may occur due to the lifting of bonding wires caused by thermal cycling.
- **Short-circuit faults**: these could happen due to wrong gate voltage (driver-circuit malfunction, failure of auxiliary power supply, etc.) and intrinsic failure (overcurrent, overvoltage, too high temperature, avalanche stress, etc.).
- **Intermittent gate misfiring faults**: these are caused by degradation of driver circuit, deterioration of control circuit, distortion of circuit elements due to electromagnetic interference, etc.

7.2 Estimation of expected lifetime of IGBT

Most of the IGBT failures are the result of excessive thermal stress, which damages the solder connection and/or lifts the wire bonds. According to [63], the internal connections of switching devices are subject to aging due to the thermal cycling, since the connected materials have different expansion coefficients. Thus, the expected lifespan of a switch can be expressed as a function of the temperature and the temperature swing. The number of cycles to failure N_f is recently used by many manufacturers to

specify the lifespan of a switch, which can be modeled by the Arrhenius relationship [6]:

$$N_f = \frac{A}{\Delta T_j^{\sigma}} \cdot exp\left(\frac{E_a}{k_b \cdot T_{j,m}}\right), \tag{48}$$

where the terms A and σ are empirical constants. $k_b = 1.38 \cdot 10^{-23} \frac{\mathrm{m^2 kg}}{\mathrm{s^2 K}}$ is the Boltzmann constant and $E_a = 0.7$ eV refers to the thermal activation energy.

Figure 75 shows typical curves of the number of cycles to failure N_f of an IGBT module as example, in which the lifespan of IGBT is plotted as function of the swing of the junction temperature ΔT_j, with the median of the junction temperature $T_{j,m}$ as parameter. The data for this figure was taken from [63].

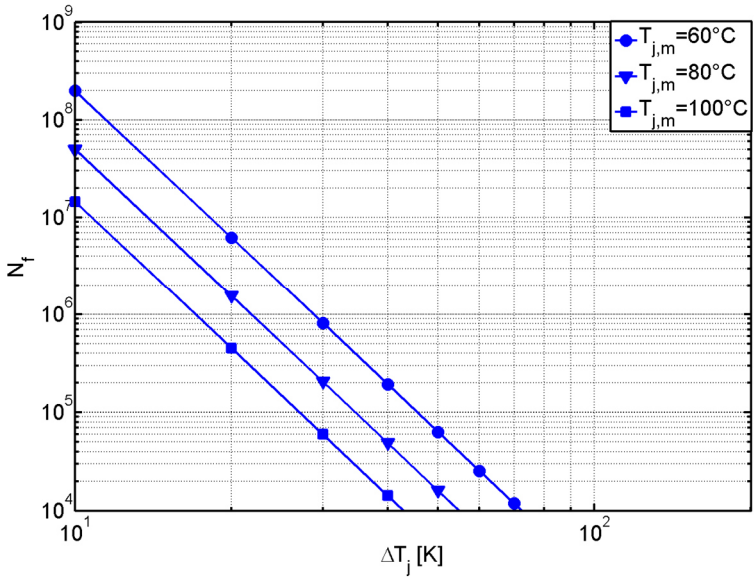


Figure 75: Typical cycling capability curves of an IGBT module. $T_{j,m}$ is the median junction temperature and ΔT_j the swing of the junction temperature

Obviously, the knowledge of the swing and of the median value of the junction temperature is necessary for the estimation of the switch lifetime. The median value $T_{j,m}$ and the average losses $\bar{P}_{Loss}$ of a switch can be estimated by means of measurement of heatsink and ambient temperature. On the other hand, the swing of the junction temperature cannot be obtained in this way, since the heatsink is characterized as a low-

pass filter having a large value of the thermal time constant. Nevertheless, the ripple can be estimated by using another approach.

It is assumed that the VSI produces sinusoidal currents, thus each switch of the inverter dissipates losses only for a half period of the load current. Therefore, the pulsating losses $P_{Loss,Pulsating}$ of a switch can be estimated from the average losses $\bar{P}_{Loss}$ by applying the formula $E_{Loss} = \int_0^{1/f_c} \bar{P}_{Loss} dt = \int_0^{1/f_c} P_{Loss,Pulsating} dt$, where f_c is the frequency of the load current [63]. The principle of the calculation is illustrated in Figure 76 for the case of a switch of the upper leg of inverter.

Obviously, the redistribution of losses among the switches of the inverter affects not only the median value of the junction temperature of each switch but also impacts the magnitude of the temperature swing.

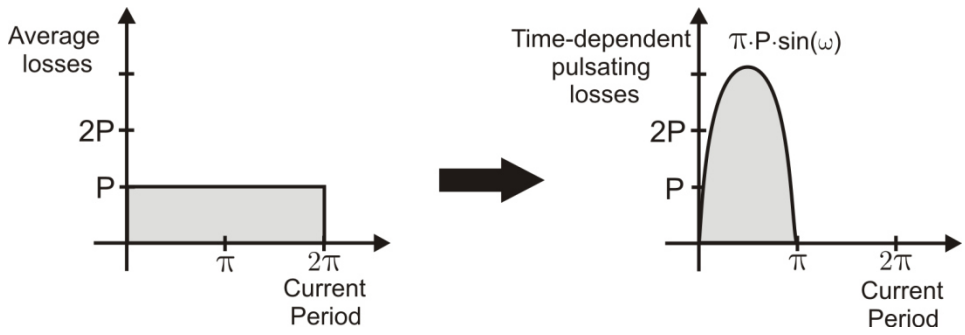


Figure 76: Calculation of pulsating losses $P_{Loss,Pulsating}$ from the average losses $\bar{P}_{Loss}$, estimated by measuring the heatsink temperature in steady state. The time dependency is approached as a sinusoid.

Figure 77 shows the results of the calculation of the junction temperatures of the used switch for two examined cases, in which the load current has the same amplitude but different values of frequency. Obviously, the case with the lower current frequency yields a higher temperature swing as to the other, although the values of median junction temperature for both cases are equal. The lifetime calculations have to consider the thermal equivalent circuit of the module with all the time constants and parameters as given by the manufacturer [63].

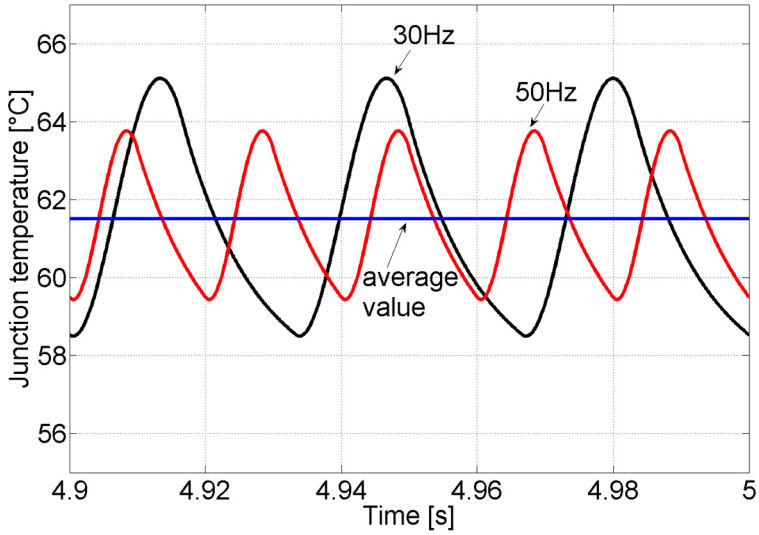


Figure 77: Simulated junction temperature of switch 1 for the two fundamental frequencies 30 Hz and 50 Hz. Both the examined cases yield the same median junction temperature

7.3 Impact of loss redistribution on expected lifespan of 3L-NPC VSI

7.3.1 Lifespan of 3L-NPC VSI

A 3L-NPC VSI consists of 12 IGBTs, which are considered as the lifetime-critical components. The neutral-point diodes are regarded as very robust and are not taken into consideration. The other components, e.g. DC-link capacitors, are not in the focus of this work. Thus the number of cycles to failure N_f^{System} of the inverter is limited mostly by the weakest switch suffering thermal overload:

$$N_f^{System} = \min(N_f^{IGBT1}, N_f^{IGBT2}, \cdots, N_f^{IGBT12}), \tag{49}$$

where $\min(.)$ is minimum function and N_f^{IGBT1},.., N_f^{IGBT12} are referred to the number of cycles to failure of each switch, which are calculated by applying equation (48). The numbering rule of the switches of 3L-NPC VSI can be seen in Figure 78.

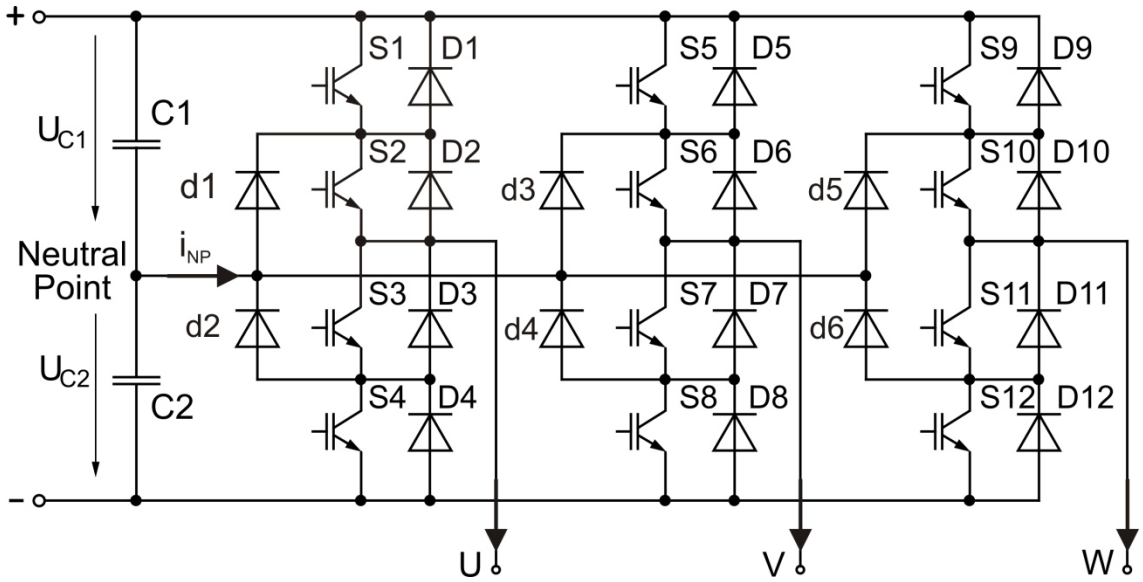


Figure 78: 3L-NPC Inverter

For the normal operation and for the range of low modulation index, the inner switches, e.g. switch 2, suffer from higher load than the outer ones, e.g. switch 1, due to the different switching patterns. As a result, the expected number of cycles to failures of the 3L-NPC VSI is limited by the thermal cycling capability of the inner switches (2, 3, 6, 7, 10 and 11):

$$N_f^{System} = \min\left(N_f^{IGBT2}, N_f^{IGBT3}, N_f^{IGBT6}, N_f^{IGBT7}, N_f^{IGBT10}, N_f^{IGBT11}\right). \tag{50}$$

The distribution of losses becomes inversed for the operation in the range of higher modulation index, where the outer IGBTs suffer under more load and become the weak components of the system. Therefore (49) is evaluated for the switches (1, 4, 5, 8, 9 and 12):

$$N_f^{System} = \min\left(N_f^{IGBT1}, N_f^{IGBT4}, N_f^{IGBT5}, N_f^{IGBT8}, N_f^{IGBT9}, N_f^{IGBT12}\right). \tag{51}$$

The operation of a 3L-NPC VSI in the low modulation index range offers many facilitations: the complete suppression of ripple of the neutral-point voltage, the ease of application of PWM with ALE, etc., because the reference-voltage space vector is synthesized using only the redundant voltage space vectors. However, the inverter is op-

erated in this range only for the starting phase. Thus, in the following, the impact of the ALE on the lifespan of the 3L-NPC VSI is examined for the high modulation index range. The investigation for the low modulation index range can be carried out in the same manner.

Switch 1 is assumed to be exposed to thermal overload and the other switches are not affected; thus, the expected number of cycles of the system $N_f^{System,F}$ is calculated as:

$$N_f^{System,F} = N_f^{IGBT1}. \tag{52}$$

It is well known from the experimental results that the switches 5, 8 and 9 suffer from higher load as the consequence of the application of PWM with ALE, especially switch 5. Thus the expected lifespan of 3L-NPC VSI by applying PWM with ALE is limited by the switches 1 and 5:

$$N_f^{System,ALE} = \min(N_f^{IGBT1,ALE}, N_f^{IGBT5,ALE}). \tag{53}$$

Now a lifetime extension factor η can be introduced, that describes the extension of the lifespan resulting from the application of PWM with ALE. The lifetime extension factor η shall be defined as:

$$\eta(\Delta P^{IGBT1}, \Delta P^{IGBT5}) = \frac{N_f^{System,ALE} - N_f^{System,F}}{N_f^{System,F}}, \tag{54}$$

where the variable ΔP^{IGBT1} is the relative reduction of losses in switch 1, which is defined as:

$$\Delta P^{IGBT1} = \frac{P_{Loss,Fault}^{IGBT1} - P_{Loss,ALE}^{IGBT1}}{P_{Loss,Fault}^{IGBT1}}. \tag{55}$$

The term $P_{Loss,Fault}^{IGBT1}$ stands for the total losses of switch 1 in the case of the occurrence of a thermal overload and no protective provision made. $P_{Loss,ALE}^{IGBT1}$ is referred to the total losses of switch 1 *after* applying PWM with ALE to relieve the switch 1.

To ease the analysis, a **worst-case scenario** is assumed in which $\Delta P^{IGBT1} = -\Delta P^{IGBT5}$ or the losses removed from switch 1 are transferred totally to the switch 5. Now, the lifetime extension factor $\eta(\Delta P^{IGBT1})$ is simply a function of ΔP^{IGBT1}.

7.3.2 Degradation of cooling system

The thermal resistance of a passive heatsink (only convection and radiation) can become **5** to **15** times larger than the same heatsink equipped with active (forced) cooling function [63]. Therefore, the thermal resistance of an active cooling heatsink R_{ha} will be increased significantly, if the cooling system does not work properly or the heatsink is placed in hot environment, which happens likely in the practice due to the placement of different switches in a small space.

In order to illustrate the benefits of PWM with ALE in case of a malfunction of the cooling system, the following case is considered: the value of thermal resistance of heatsink of switch 1 is assumed to increase by 100% as a result of degradation of the cooling system and the inverter is operated with modulation index $m = 0.95$ at full torque.

The results of different calculations of N_f are shown in Figure 79. The columns in green depict the number of cycles N_f of the examined switches and of the inverter for normal operation. The lifetimes of the switches and of the total system in case of the occurrence of thermal overload are depicted in red.

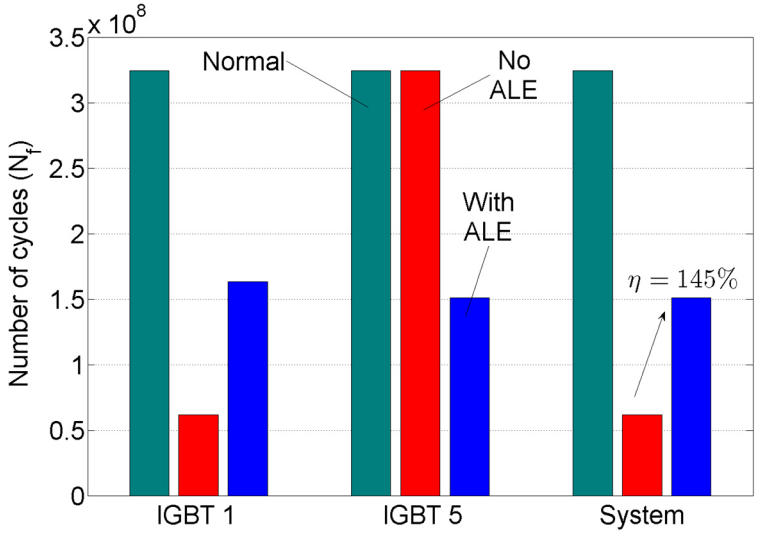


Figure 79: Impact of cooling system failure and transfer of loss of switch 1 to switch 5 on the lifetime of the inverter; m = 0.95 at full torque

It can be seen that, the expected lifespan of switch 1 is reduced significantly and it is much smaller if compared with that of switch 5. PWM with ALE is set to transfer 10% of the total losses of switch 1 to switch 5, which is notated as $\Delta P^{IGBT1} = 0.1$. As a result of the relief, the lifetime of switch 1 is improved considerably at the cost of a reduction of the lifetime of switch 5. Actually, switch 5 results to be the weakest component of the system instead of switch 1; however the lifespan of the total system is increased by 145% or the extension factor $\eta(\Delta P^{IGBT1} = 0.1)$ equals 1.45 thanks to the load redistribution among the switches

The effectiveness of ALE will be further investigated for different values of ΔP^{IGBT1} with two overload scenarios, in which the values of the thermal resistance of the heatsink of switch 1 are assumed to be increased by +50% and by +100%.

Figure 80 shows the effect of the application of PWM with ALE on the lifetime extension of the inverter with respect to the loss reduction of switch 1 ΔP^{IGBT1}. Here, the inverter is operated with rated torque for different modulation indices m, but the influence of m is small.

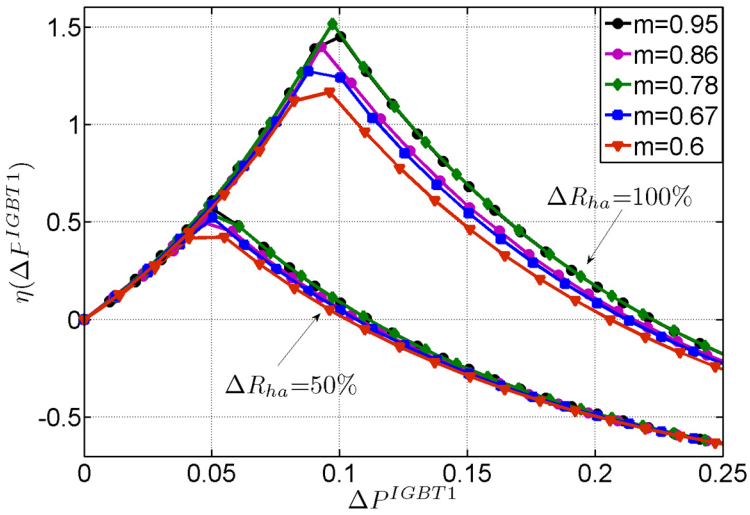


Figure 80: Lifetime extension factor $\eta(\Delta P^{IGBT1})$ for the case of malfunction on the cooling system, torque equals 100% rated value

For each examined scenario, the lifetime extension factor $\eta(\Delta P^{IGBT1})$ reaches the maximum value for $\Delta P^{IGBT1} = \Delta P^{IGBT1}_{Optimum}$, where the expected lifetimes of switch 1 and switch 5 are almost equal. It means, the larger the lifetime difference between switch 1 and switch 5 or the more severe the degradation, the larger amount of losses of switch 1 is required to be transferred to switch 5.

If ALE is applied such that $\Delta P^{IGBT1} > \Delta P^{IGBT1}_{Optimum}$, switch 5 becomes the endangered component instead of switch 1, the effectiveness of the ALE strategy declines. Furthermore, such operation causes higher distortion of the neutral-point voltage, since PWM with ALE has to be applied to a longer period, to achieve a larger reduction of losses in IGBT 1. Therefore, it is strongly recommended to operate the PWM with ALE so that $\Delta P^{IGBT1} < \Delta P^{IGBT1}_{Optimum}$, to achieve the best tradeoff between lifetime extension and control quality of the neutral-point voltage.

Obviously, the optimum value $\Delta P^{IGBT1}_{Optimum}$ depends strongly on the change of the thermal resistance of the heatsink ΔR_{ha}. This can be determined by sensing the heatsink temperature of each switch, which is consequently compared with the reference value saved in a look-up table. Such a look-up table is to be constituted from the measurements of the heatsink temperature for different operating points in *normal condition,* with regard to different modulation indices and to different values of torque. A large

deviation of the actual value from the reference value indicates the occurrence of the degradation and is directly proportional to the value of ΔR_{ha}. Since this strategy for the detection and the determination of the degradation is very simple, it can be easily implemented in practice.

The calculations of different scenarios show that a significant improvement of the lifetime of the inverter can be achieved, if ALE is properly applied in case of thermal overload. A lifetime extension factor up to 150% can be obtained for the worst-case scenario, in which it is assumed that the total losses are transferred from switch 1 only to switch 5. In fact, the thermal load is redistributed among the switches 5, 8 and 9, thus the lifetime extension of inverter is expected to be higher than in the worst case, a larger amount of losses can be distributed among the other switches and not only transferred to switch 5 as in the worst case.

8 Conclusion

The main objective of the presented work is the study of the utilization of redundancies in the switching states of a three-level NPC inverter for the distribution of the losses among the switches of the inverter. Usually the redundancies are exploited for the control of the neutral-point voltage of the DC link, but as proposed in this work they can be utilized for the redistribution of losses among the power semiconductors of the inverter as well. In case of a failure of the cooling system of a switching device, it can thermally be protected by transferring its losses to the other switches that still have a well-functioning cooling. In this way, the further operation of the inverter until repair is feasible and an extension of the lifetime of the whole system even in the presence of local hotspots can be achieved. Therefore, the proposed fault-tolerant strategy is called active lifetime extension (ALE).

For the achievement of the defined objective, the thesis presents two approaches for the modification of the switching schemes of a 3L-NPC VSI by utilizing the redundant switching states. The first approach focuses on the modification of the switching patterns of a Space-Vector Pulse Width Modulation (SV-PWM) and of a Discontinuous Pulse Width Modulation (D-PWM) scheme, which are characterized for good DC-link voltage utilization, excellent capability to modify the switching pattern, etc. Here, SV-PWM has been further improved for the ease of practical implementation.

Thus in the frame of this work, the development and implementation of a modified PWM with ALE for the redistribution of losses in a particular overheated switch have been successfully carried out. In order to achieve the goal of the investigation, the conventional switching patterns were modified taking into account the point of operation, the kind of losses affected by each pattern, i.e. conduction or switching losses, and the stability of the neutral-point voltage of the inverter. Furthermore, for obtaining an optimum result, operational maps are proposed for the implementation of modified PWM with ALE that are designed by considering the restrictions mentioned above, especially the modulation index in the point of operation and the neutral-point voltage.

The effectiveness of the developed switching schemes in transferring the losses from one switch to the others has been verified by means of simulation and of laboratory measurements on a dedicated setup.

Due to the importance of Direct Torque Control (DTC) in AC drives, the second approach considers the application of the same idea in a DTC scheme. For this purpose, the sectors of the switching table of the DTC are modified to permit the active loss redistribution among the switches. This scheme has been verified only by means of simulation because of the expenditure of implementation and the limited time.

Finally, the impact of loss redistribution on the expected lifespan of an inverter is considered. This investigation shows that in case of thermal overload of one switch only a small amount of losses is required to be removed from the affected device to the others, and the expected lifetime of inverter can be extended up to 150%.

Further works should consider the utilization of the proposed modified PWM in a closed control loop that monitors the temperature of the heatsinks of the switches.

9 Appendix

9.1 Parameters of lab drive system

3L-NPC VSI	U_{DC}	**560 V**
	C_{DC}	**4,4 mF**
	I_{rated}	**37 A (rms)**
	$f_{switching}$	**5 kHz**
Induction machine (ABB M2AA160L4)	P_{rated}	**15 kW**
	U_{rated}	**400 V**
	I_{rated}	**31,1 A (rms)**
	n_{rated}	**1455 min^{-1}**
	M_{rated}	**98 Nm**
	p	**2**
	$\cos \varphi_{rated}$	**0,78**
IGBTs for 3L-NPC VSI (IXYS IXGR72N60A3H1)	V_{CE}	**600 V**
	V_{GES}	**±20 V**
	$V_{CE,sat}$	**1,45 V**
	$I_{C,110}$	**52 A**
	$I_{F,110}$	**32 A**
	$R_{th,jc}$	**0.62 K/W**
	$R_{th,ch}$	**0.2 K/W**
	$R_{th,ha}$	**1.1 K/W**
	$C_{th,jc}$	**0.01797 J/K**
	$C_{th,ha}$	**421 J/K**
	T_{JM}	**150 °C**

Table 9-I Parameters

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